RESEARCH ARTICLE

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Implementation of Low Power DFT for ASIC SOC

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ABSTRACT

In System on Chip (SoC), a low power DFT technique plays a crucial role to reduce power consumption. These low power techniques throw a major challenge for the designers and verification engineers. Different low power DFT techniques like multiple Supply Voltages, Power Switches, clock gating, low power isolation cells and so on are applied at various stages of DFT flow. In this brief, the primary focus is to reduce the dynamic power consumption of a digital circuit in the scan Synthesis phase. Here a common clock is connected to all scan flip-flops with a frequency of 40MHz.Without any timing violations, the clock frequency is reduced to 20MHz thereby ensuring that there is a reduction in dynamic power consumption to a value of 50%.

Key Words: Low power, DFT (Design for Test), Scan Flip-flops, Supply Voltages, Power Switches, clock gating, low power isolation cells.

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INTRODUCTION

With increase in VLSI technology, handling power issues in ASIC/FPGA design have become more challenging. Also, power challenges faced by the designers are quite complex. When testing complex SoC's, designers require more testing time to test high amount of testing data and its corresponding memory. Similarly, designers should work on Low power Design Techniques at testing mode just as at the practical method of the plan. With the expansion in the unpredictability of Integrated Circuits, the bite the dust size constantly diminishes thereby clearing the path for the force utilization to be a significant angle at the utilitarian stage as well as at the assembling stage. The following are the important factors at the functional stage of SoC that implies to higher power consumption:

- Designing at higher levels
- Packaging and Cooling requirements
- Lesser device reliability
- Smaller battery life

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In this way, it is imperative to spare the force in the unused pieces of the chip. A System on Chip, integrates any number of intellectual properties. Each and every IP has its own power specifications and requirements. As examined SoC is incorporated with numerous IP's the absolute intensity of the chip is expanded to an incredible degree, which thus may prompt the disappointment of SoC's capacity the board framework. To defeat this impact, each IP is principally isolated into various force areas and they can be killed and on [1-3].

Common ASIC design flow

An average ASIC configuration stream has the accompanying succession of steps. The common ASIC configuration stream is exhibited in Figure 1.

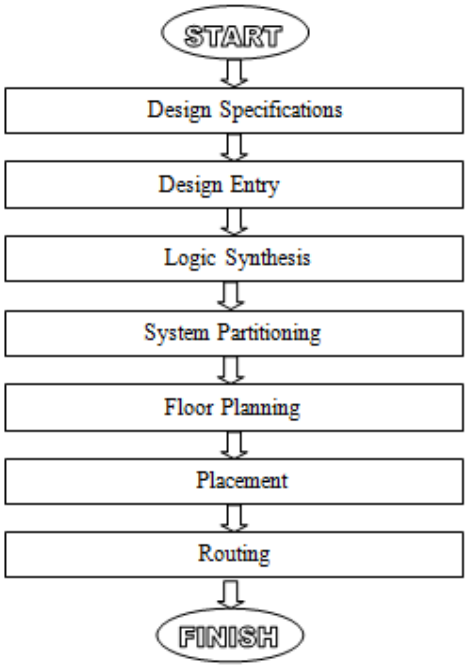

Figure 1: Common ASIC Design Flow

Design Specifications: The requirements that are needed for the design are listed.

- Design entry: The plan is coded either in Hardware Description Languages (VHDL or Verilog HDL) or Schematic is drafted.
- Logic Synthesis: Conversion of HDL code into target primitives in terms of netlist – which is a combination of logic cells and their interconnections.
- System Partitioning: Dividing a large system into equal-sized partitions.
- Floorplanning: Arranging the logic blocks of the netlist.
- Placement: Deciding the locations of logic cells inside the logic block.
- Routing: Establishing the connections between logic blocks and logic cells.

DFT Design flowing ASIC

The flow diagrams of ASIC Design flow until the Design for Test phase is shown in Figure 2.

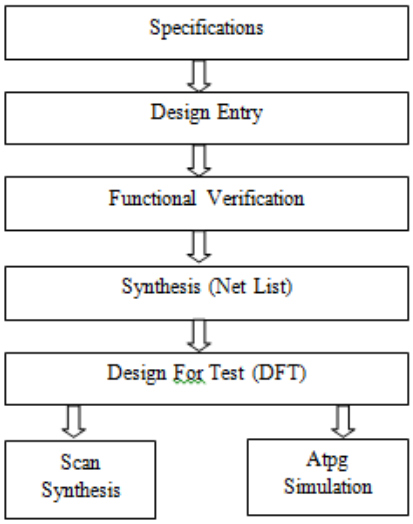

Figure 2: DFT Design flow in ASIC

From the above DFT based ASIC Design Flow, it is evident that the DFT stage starts once the netlist is generated after the completion of the synthesis step [4,5,6]. Additionally from figure 2, we can realize that low force DFT procedures can be actualized in two stages:

- Scan Synthesis Phase [1]
- ATPG Simulations Phase [1]

Scan Synthesis Phase

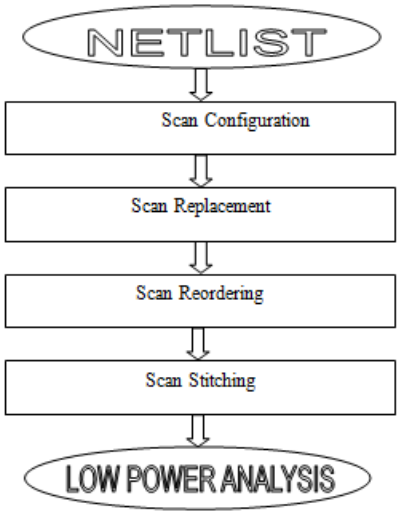

Figure 3: Flow chart of Scan Synthesis Phase

The different steps involved in scan synthesis phase are shown in terms of a flowchart in Figure 3.

ATPG Simulations Phase

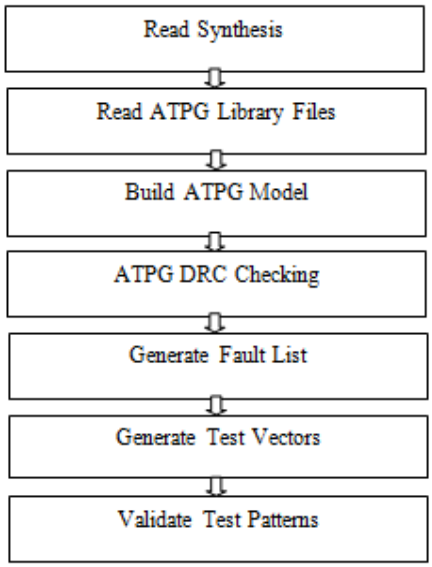

Figure 4: Flow Chart of ATPG simulation phase

The steps engaged with Automatic Test Pattern Generation (ATPG) reproduction Stage is appeared in Figure 4.

Power Saving Formats in DFT

Powers-saving formats in ASIC design are used at different levels. Most commonly used power saving formats in industry are:

- Common Power Format [7]
- Unified Power Format [7]

Common Power Format design flow had been developed by cadence and later contributed to si2. Similarly Unified Power Format had been developed using Synopsis EDA tools and has been extensively tested on 90nm and 28nm synopsis GDK libraries.UPF is mainly followed by Mentor Graphics, Synopsis and Magma. One has to remember that there is a very little difference between both power formats [7,8].

DIFFERENT LOW POWER DFT TECHNIQUES

- There are diverse low force DFT procedures utilized in ASIC and FPGA configuration streams, among them coming up next are ordinarily utilized techniques[9].
- Power Domains: The architect needs to set up the plan into different force spaces and guarantee that each square can be autonomously fueled now and again by utilizing power switches.
- Multiple Supply Voltages: Different flexibly voltages are needed at various working conditions for applying to control space blocks and these squares are associated with one another utilizing level shifters.
- Low Power Cell: The significant capacity of State Retention (SR) register is to hold the state for approved the test when power area is turned off. The low force disengagement cells are available in the middle of the limits of two force area for disconnecting power areas on and off.
- Power Switches: Power switches are primarily used to in low force plans for limiting spillage power scattering particularly brought about by contracting innovations. Force switches are utilized at better places in the plan to empower the use of intensity gating.
- Clock Gating Circuitry: In this strategy clock is turned off when it isn't practically utilized. As the constant exchanging of check in the middle of 0's and 1's burns-through a decent measure of dynamic force. Turning off the check at whatever point not being used encourages the originators to spare the power. It is a method for diminishing force utilization in a force on space by powerfully hindering the clock to arrive at a bunch of consecutive components. Power-Aware DFT:
- During the scan synthesis, functional flip-flops used in the design are replaced by equivalent scan flip flops. In the process of scan synthesis, power aware DFT is used to partition the scan chains with the condition that there are required scan I/O's , control signals and dedicated test clocks at each power domain. This ensures that each power domain has dedicated scan chains that are active in the power modes in which this domain in ON.

Implementation of the Low Power DFT Techniques

In this brief, for executing low force DFT strategies, we have set the SCAN check recurrence so that the plan determinations are met and furthermore the

force utilization of the circuit is decreased to a degree. For executing this, we have taken an advanced PLL with various tickers as an information plan. The door level net-list produced after blend is a contribution for the DFT cycle and on a similar net-list low force DFT procedures are actualized by diminishing recurrence of SCAN clock.

The nonexclusive portrayal of a CMOS rationale entryway for Switching Power Calculation is portrayed in Figure 5:

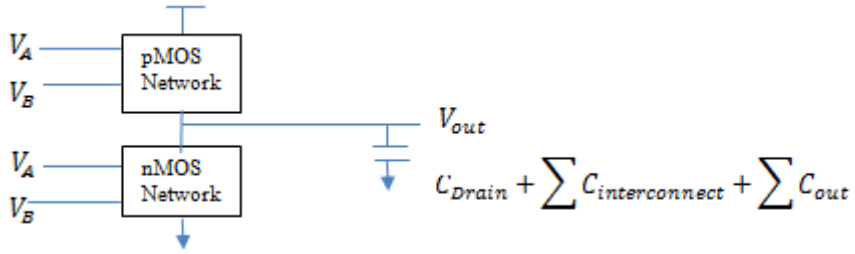

Figure 5: Representation of switching power calculation in CMOS logic gate.

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} Vout \quad (-C_{out}\frac{dV_{out}}{dt})dt + \int_{T/2}^{T}(V_{DD} - V_{out})(C_{load}\frac{dV_{out}}{dt})dt\right] \tag{1}$$

The average power consumption is

$$P_{avg} = \frac{1}{T}C_{load}V_{DD}^2 = C_{load}V_{DD}^2 f_{CLK} \tag{2}$$

$$P_{avg} = \propto_T C_{load}V_{DD}^2 f_{CLK} \tag{3}$$

Where (α_T) is node transition factor.

Therefore generalized expression for the average power dissipation is

$$P_{avg} = \left(\sum_{i=0}^{\#ofnodes} \propto_{Ti} C_I V_i\right)V_{DD}F_{CLK} \tag{4}$$

From Equation 4, Power is straightforwardly corresponding to the clock recurrence. Consequently, diminishing the clock recurrence with the end goal that it falls between the detail runs, the force can be decreased without influencing the circumstance infringement in this way.

RESULTS

The test results are completed in Synopsis DFT apparatuses at the Scan Synthesis level, by differing the clock recurrence. Initially, here a clock with a recurrence of 40MHz is applied to all the sweep flip-flops in the plan and relating power boundaries are determined. Later the clock recurrence is diminished to 20MHz and the clock is applied to all the output flops. The relating power boundary esteems are

Table 1: Different Power Parameters

Power Type	Before applying the low power technique	After applying the low power technique
Cell Internal Power (CIP)	1000 uW	**510 uW**
Net Switching Power (NSP)	154 uW	**77 uW**
Cell Leakage Power (CLP)	99000 uW	**99000uW**
Total Dynamic Power(TDP)	1200uW	**588 uW**

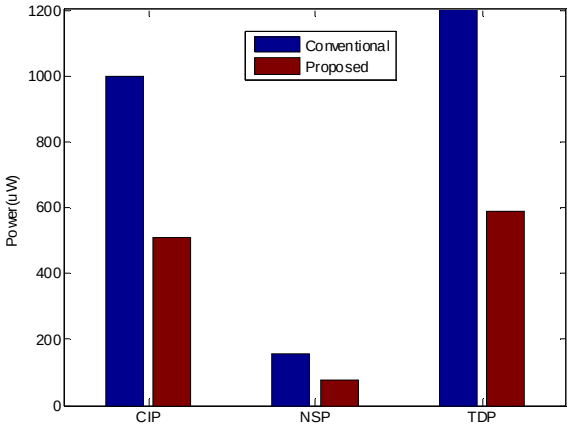

Figure 6: Different Powers comparison

determined. Likewise, any of low force innovation is utilized to diminish the force. The distinctive force boundaries esteems when applying power esteems are appeared in Table 1 and figure.6. From the table, it is apparent that absolute unique force is diminished to half of the force burned-through when the recurrence is decreased to half of the recurrence.

CONCLUSION

From the above outcomes, it is clear that the dynamic force is dispersed roughly by an estimation of half when the clock recurrence is diminished to 20MHz from 40 MHz. Here the force utilization esteems are taken so that there no arrangement and hold timing infringement in the circuit subsequent to decreasing the recurrence. From this, we can say that force is legitimately relative to recurrence. The fashioners can likewise apply the procedure of isolating the SCAN clock for odd and even anchors to diminish power scattering.

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