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Ultra-Low Power Stacked nMOS m-Sequence Code Generator with Reduced Leakage Power for Body Sensor Node Applications

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ABSTRACT

The rapid increase in population which is itself leading to a varied type of diseases is throwing a challenge to the medical technology nowadays. Body Sensor nodes (BSNs) are the devices which are used for the real time monitoring of the patient's condition. These BSNs were very helpful in exact analysis of the condition of the patients without any kind of the physical operation. The BSNs thus has to work efficiently for the outmost applications. The power consumption of such devices comprises of many factors which includes leakage power. The leakage power can be reduced using the stacking technique. In this paper, nMos stacking technique is used to reduce the leakage power of m-sequence code generator which is the main block in transmitter of BSN. Such reduction of the leakage power will lead to increase in the energy efficiency of the BSN. 90nm CMOS technology is used to simulate the proposed m-sequence code generator. The simulation results have shown that the proposed m-sequence code generator has less average power by having less leakage power.

Keywords: Body Sensor Node, m-sequence code generator, Stacking technique, Power consumption.

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INTRODUCTION

The body sensor nodes are basically the devices used to transmit the data from the human body into the physical environment by means of the wireless or wired medium as shown in Fig.1. These body sensor nodes work at lower voltages and with low power supply, but these must be continuously supplied with the power in order to have real time observation. In this scenario the power consumption of the device will make an enough impact on the performance and feasibility (since more power consumption requires more amount of the supply power which leads to the more number of batteries or frequent replacement of them).

The BSN in the whole comprises of a sensor which is used to sense the information from the patient by some means, the sensed information has to be sent to the desired destination. This can be done with the help of transmitter. The transmitter itself comprises of an m-sequence code generator which is used to produce a pseudo code in order to achieve the spread spectrum technique. The spread

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spectrum technique is used to spread the original data into a wider range. This technique is used in case of the multi-user scenario [1]. Apart from this, the BSN will also comprise a receiver part which is used to extract the original signal by some demodulating techniques.

Much advancement has been done in this field in order to reduce the power consumption. Some of the major advancements involve the usage of the CMOS technology which reduced the power consumption to a great extent and made the design to work under low supply voltage, another method involves the scaling of the supply voltage [3]. This made the design to work in a very efficient manner. The main concern in these advancements is that they reduce the switching frequency of the circuit. But in case of the medical field, this reduction in switching frequency can be trade off [4].

The earlier studies concentrated in the reduction of the power consumption in the m-sequence code generator to a great extent [2]. The leakage power is also responsible for the power consumption of the design, so the reduction in the leakage power will leads to the significant reduction in the power consumption.

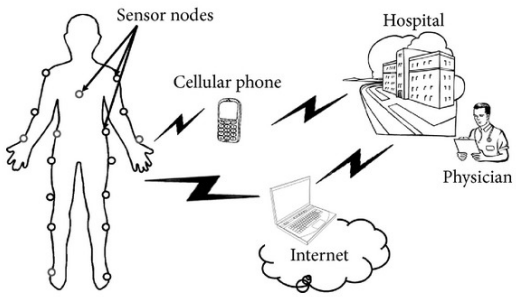

Figure 1: Examples of medical applications of BSNs

Hence in this paper, a new m-sequence code generator design has been proposed with the help of the stacking technique which reduces the leakage power of the design and made the design to work effectively and produce the exact output even at sub-threshold levels.

The contributions of this paper are summarized as follows:

1) Leakage power is calculated for the designs with only transmission gate [T.G] are being stacked.
2) And then the design with T.G and inverters being stacked.
3) Finally the design in which T.G, inverters and NAND gates being stacked.
4) Comparison of leakage powers in all these three cases was done.

M-SEQUENCE CODE GENERATOR

The sequence which has to be generated by the m-sequence code generator has an vital contribution in the power consumption, toggle rate is a factor which is responsible for the number of toggles in the sequence generated. This paper is more concentrated on the single user usage, so the sequence which is to be generated by the m-sequence code generator is considered as a 7-bit code with the sequence '1001110' [1]. The toggle rate of this code is found to be 0.42 which is less than the recommended value 0.45.

The typical m-sequence code generator consists of a linear feedback shift register (LFSR) and an feedback element which is typically an XOR gate. This whole design produces an cyclic code. For the required sequence i.e; 1001110 we required 3 D-FlipFlops and an XOR gate as an feedback element which are connected as shown in Fig.2.

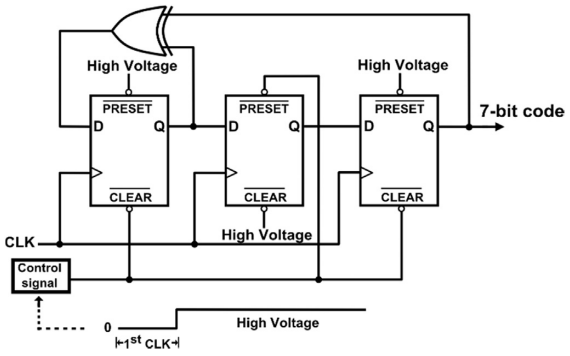

Figure 2: Block diagram of m-sequence code generator

The control signal has to be given with the initial clock pulse as 0 and the rest as 1(high) in order to produce the desired sequence. The control signal triggers the flip flops accordingly in order to produce the desired sequence.

THE STACKING TECHNIQUE

One can reduce the power consumption of the circuit either by reducing the supply voltage which can leads the increase in the delay of the circuit or by reducing the threshold voltage which also have an drawback of exponential increase in the leakage

power [7]. The leakage current is the current which is passed through the transistor when the transistor is in OFF state. This kind of scenario generally exists when the technology used is less than the 180nm.

Stacking is generally referred as the arranging two or more transistors in series instead of one transistor. The stacking can be generally done to nMOS, pMOS or both combined [8]. In this paper we have preferred nMOS stacking only.

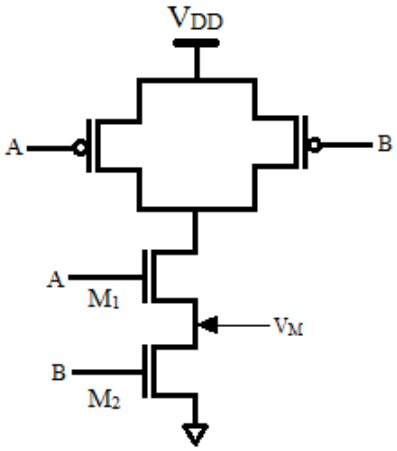

Figure 3: Representation of Stacking

Consider the above network shown in Fig.3 [9], when there is no stacking, i.e; only one nMOS device is OFF say M_1 , the voltage at the source node will be zero since remaining ON transistors were short circuited, this causes no self biasing effect and thus causes increase in leakage current at OFF transistor.

But when the stacking technique is provided for the circuit, both the transistors will be turned OFF at once and the voltage at the node V_M is positive due to the small drain leakage current which leads to the following effects:

1. Due to the positive potential at V_M, the gate source potential of the transistor M_1 becomes negative thus the leakage current reduces.

2. Also due to V_M being positive, the drain to source potential of the transistor M_1 reduces, increasing the threshold voltage of M_1 and thus reducing the leakage current.

PROPOSED STACKED M-SEQUENCE CODE GENERATOR

In this paper, the m-sequence code generator is subjected to stacking i.e the nMOS is stacked with the one that is presented in the circuit. The process is first applied only for the transmission gate, next for the inverters and in final the whole circuit is stacked.

The m-sequence code generator shown in Fig.2 comprises of XOR gate and D-FlipFlops. As D-FFs are the power consuming blocks in the m-sequence code generator, the stacking concept is applied to D-FFs.

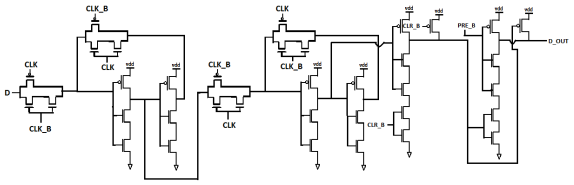

Figure 4: Schematic of Stacked D-FlipFlop

In the stacked version of the D-FlipFlop only the nMOS were stacked i.e only the nMOS transistors were arranged in series with the existing one in the design. Then the stacked nMOS D-FF is used to reduce the leakage power in m-sequence code generator which is as shown in Fig.4.

The complete stacked version of the m-sequence code generator consists of the stacked D-FlipFlops, XOR gate. The design of the completely stacked m-sequence code generator is as shown in Fig.5.

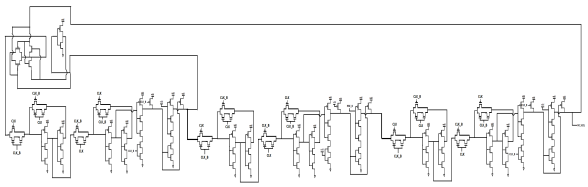

Figure 5: Schematic of Stacked m-sequence Code Generator

SIMULATION AND RESULTS

The above circuit has been simulated in the 90nm CMOS technology using cadence virtuoso. The above design is first simulated with only T.G.Gate being stacked, and the leakage power and the average power were calculated. Later the inverters in the design were also stacked along with the T.G.

Gate and at the end the whole circuit is stacked with nMOS transistors and the leakage power and average power were calculated.

From Table 1 it can be observed that the proposed fully stacked circuit has less leakage power at all the supply voltages when compared to stacked T.G only and stacked (T.G + inverter) m-sequence code generator.

The existing m-sequence code generator designs without stacking [1-2] are then compared with the proposed stacked m-sequence code generator in terms of the leakage power and average power. The results were graphically represented in Fig.6 and Fig.7. respectively. The proposed design significantly reduced the leakage power and the average power was also reduced to some extent.

Coming to the average power, since the leakage power of the proposed design has reduced a lot when compared to the previous design, the average power of the whole design has reduced significantly. The reduction in the power has shown a significant mark only when the complete design is stacked and in the remaining cases, the reduction in power is not up to the mark. Hence the proposed circuit with fully stacked nature has less average power as it has less leakage power.

One of the other advantage with the stacking technique is observed that the circuit is able to generate the sequence with the most accuracy even at the low voltages which is not observed in the case of the existing m-sequence code generators [1-2].

Table -1 : Leakage power [nW] of proposed nMOS stacked m-sequence code generator

Voltage applied	Stacked T.G.gate	Stacked T.G.gate +inverter	Fully stacked circuit
0.5V	25.67	13.52	12.02
0.6V	41.67	20.21	16.21
0.7V	65.96	29.92	21.78
0.8V	101.6	43.16	29.37
0.9V	152.3	60.14	39.89
1.0V	226.2	84.23	54.31
1.1V	333.33	118.2	73.81
1.2V	487.1	165.5	100.4
1.3V	706.6	231.0	136.7

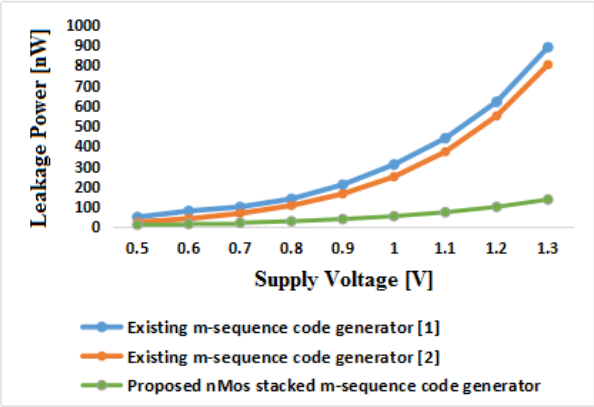

Figure 6: Leakage Power Comparison

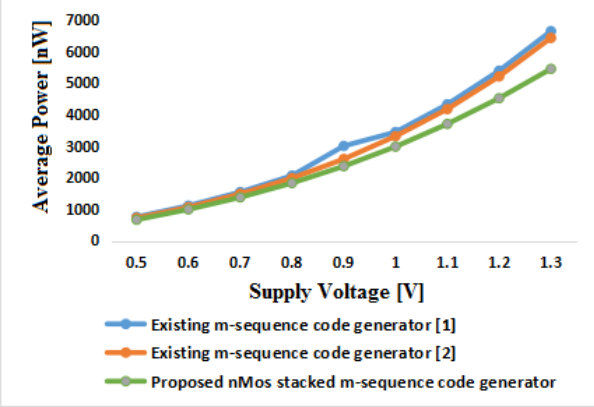

Figure 7: Average Power Comparison

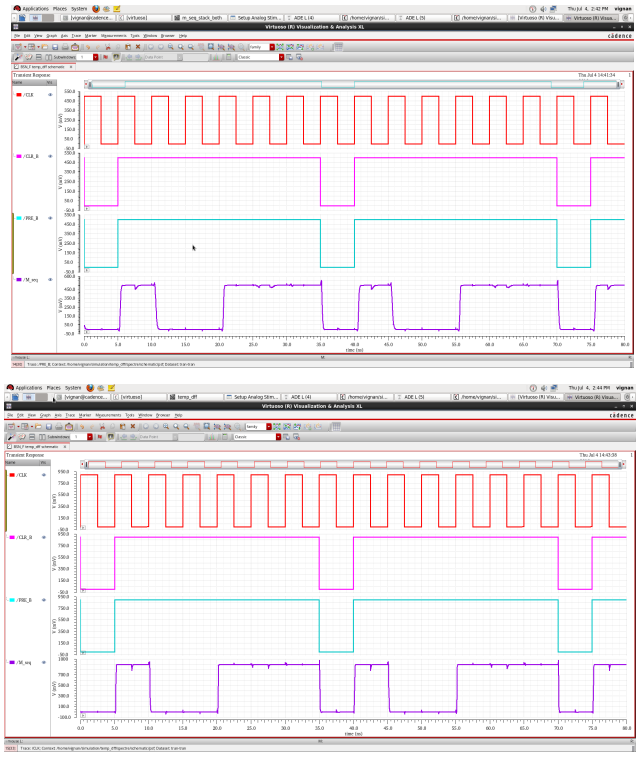

Figure 8: Transient response of stacked m-sequence code generator at supply voltage of 0.5V and 0.9V.

The transient responses of the m-sequence code generator at supply voltages of 0.5V and 0.9V are shown in Fig.8. Transient response consists of two cycles of m-sequence code 1001110 and a code bit 1 corresponding to third cycle of m-sequence code. From Fig.8 it is clear that the design is capable of producing code even at low voltages like 0.5V.

CONCLUSION

The reduction in power consumption in any manner has been concerned more in case of the digital circuits, specifically in the case of the BSNs where power consumption is a big deal to be dealt with. The leakage power is thus an important factor that has to be reduced in order to decrease the average power consumption. Hence in order to reduce the leakage power, nMOS stacking technique is used. With this nMos stacking technique, the leakage current is reduced by making gate to source voltage negative and drain to source voltage positive. The proposed circuit has been simulated using 90nm CMOS technology for various stacking levels in the circuit. The comparison has shown that the proposed fully stacked m-sequence code generator design has the least leakage power which also significantly reduced the average power of the design.

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