Various Logically Optimized D Flip Flop Circuits- A Comparative Study in Submicron Technology

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ABSTRACT

D-Flip Flop (D_FF) is a very important component of various digital, analog and mixed signal systems and designs. It is obvious to come up with optimized D_FF, that cater the needs of low leakage power, less power dissipation, less chip area on the chip and low delays. This paper presents a comparative study of various logically optimized circuits of D_FF using 8T, 11T, 12T and conventional 18T D_FF. The simulation, test circuits, schematics & layouts etc are done on Cadence Virtuoso tool in 180 nm technology. Designs are compared on grounds of power dissipation, leakage power, delays and power delay product.

Keywords—*D-Flip Flop, Leakage power, Optimization, Power Delay product, PR boundary.*

1. INTRODUCTION

The memory elements used in clocked sequential circuits are called flip flops. These circuits are binary cells capable of storing one bit of information. A flip flop circuit has two outputs, one for the normal value and one for the compliment value of the bit stored in it [1]. The way in which binary information enters a flip flop gives rise to different type of flip flops. Flip flop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states.

The D-Flip Flop is a modification of basic clocked RS flip flop such that the D input directly goes to the S input and its compliment is applied to the R input. The D input is sampled during the occurrence of a clock pulse. The D flip flop receives the designation from its ability to transfer "data" into a flip flop. It is also expanded as Delay Flip Flop.

The analysis of excitation table of D flip flop shows that D must be 0 (zero) if Q(t+1) has to be 0 (zero) and D must be 1 (one) if Q(t+1) has to be 1 (one) regardless the value of Q(t) [2]. The excitation of D flip flop is shown in Table-1.

Table 1: Excitation Table of D Flip Flop

D	Q(t+1)
0	0
1	1

D Flip Flop is one of the important digital circuit which has enormous applications in various digital design. This the age of fabricating the digital and analog circuits on ICs using CMOS technology. CMOS is most promising technology among available techniques. Among various advantages associated with this technique the most important is its low power dissipation feature. Whether digital systems are high speed, high density, low power, or low cost, CMOS technology finds ubiquitous use in the majority of leading edge commercial applications [3].

Digital CMOS circuits dissipate power in three ways due to signal transition, due to short circuit

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currents and due to leakage currents [4]. Delays depend on many factors like supply voltage, threshold voltage, aspect ratio, oxide thickness and load capacitances [5].

Low power design with high performance for battery operated portable systems, is a strong direction for CMOS system design. The power dissipated by a CMOS circuit (P_{TOTAL}) is the sum of the static power (P_S), the dynamic power (P_D), and the short circuit power (P_{SC}). i.e.

$$P_{TOTAL} = P_S + P_D + P_{SC}$$

Ps may be reduced to that due to leakage, if any circuits that draw DC power such as pseudo NMOS circuits are eliminated. The dynamic power is dependent on the supply voltage, the stray capacitances, and the frequency of operation. The reduction in supply voltage is quadratic while the speed is inversely proportional to supply voltage [6,7]. The stray capacitances may be reduced by using smaller no. of transistors to implement a function [6]. The essential thing in CMOS design technique is that it should maintain the performance while achieving the low power [6].

In this paper based on the theory of logic optimization different optimized circuits for the D Flip Flop have been studied. The theory of logic optimization is employed here to achieve the targets of low power and low delay for these circuits. The theory of logic optimization is explained in detail in next section i.e. section II. As examined in the Section V (Results and Conclusion) the desired objectives are achieved.

Section III is dealing with most important aspect of this paper that is actually what has been done actually in various optimized circuits. In Section IV relevant layouts, schematics, and waveforms are shown concerning with different optimized circuits.

2. CONCEPT OF LOGIC OPTIMIZATION

The implementation of optimization involves synthesis of logic function and techniques for deriving minimum cost implementation of logic function [8]. Key to find a minimum cost expression for given logic function is to reduce the no. of terms needed in the expression by applying the combining property [9].

The task of logic design/redesign/optimization is to combine (many) signals arising at various locations and points in time to (few) signals desired at various locations and points in time via a logically non-trivial structure. We focus on the "many" to "few"= 1 case, i.e redesign of critical paths [10]. The process of logic optimization involves, improving the algorithm to be implemented with respect to signal locations, using complex gates, bridge distance with inverter trees, avoidance of cloning, gate sizing, blockages, and better delay model.

The level of abstraction of high-level synthesis does not allow accurate estimates of the figures of merit of a circuit. Consequently, a straightforward mapping of an RTL design into a logic circuit very seldom meets area, speed, or power requirements. Optimization at the logic level is therefore a necessary step: indeed, its relevance has made it the subject of intense research ever since the inception of electronic computers [11].

The property of regularity extraction is somewhat employed to achieve efficient optimization of the circuits [12]. Several techniques for extraction of regularity are there. Many of these techniques focus on functional regularity by matching the circuit with templates [13, 14, 15], it has rarely been used in the logic optimization of a design. To make use of this important property, it is necessary to extract functionally equivalent parts of a design.

Logic optimization inherently involves timing optimization. In timing optimization, we concentrate

on the three most important topics: repeater trees, logic restructuring, and choosing physical realizations of gates (sizing and V_t-assignment). These are the main components of Bonn Opt, and each uses new mathematical theory [16] .

3. WORKING PROCESS AND PARAMETERS

Based on the above cited theory of logic optimization, in this paper four popular logically optimized D flip flop circuits are studied. Certain changes have been made in these circuits with respect to the total width, finger width, number of fingers and aspect ratio of the component PMOS and NMOS [17]. The optimized circuits are using 8 transistors, 11 transistors, 12 transistors and 18 transistors. The design using 18 transistors is composed of PMOS and NMOS with total width of 2u each and rest of the parameters as usual. The design using 12 transistors is composed of 6 PMOS having total width of 4u each, 2 PMOS having total width of 2u each and 4 NMOS with total width of 2u each, the finger width of each of these transistors are set equal to 1u and number of finger will be set automatically by the tool. The design using 11 transistors is composed of 5 PMOS with total width of 4u each, 2 PMOS having total width of 2u each and 5 NMOS with total width of 2u each, the finger width for 5 PMOS with total width of 4u is equal to 2u and for rest of the transistors the finger width is set equal to 1u. 8 transistors D flip flop is composed of 2 PMOS with total width equal to 6u, 4 PMOS with total width of 3u and 2 NMOS with total width of 3u, finger width for all of these transistors is set equal to 1u.

The gate width or simply the width of a transistor can be thought of as the number of parallel channels that are available for current to pass from the source to drain [18]. Number of Fingers means number of poly gate stripes used in layout. Width Per Finger or finger width means width of each gate stripe [19]. If width is set equal to say 4u and no. of fingers are 2 then finger width of each of these finger will be equal to 2u that will be set automatically by the tool. This can easily be inferred from the layouts shown in the paper.

The layouts and output waveforms of these circuits are shown below and the relevant results pertaining to these circuits are tabulated in the following tables . The results will be compared and discussed later in this paper. As the output waveforms of all the designs are similar, hence for the sake of economy of space only one of the output waveform of most optimized design is presented in this paper.

4. SIMULATIONS

The following figures are the actual schematics and layouts that actually have been simulated in Cadence Virtuoso tool in 180 nm technology i.e. submicron technology. Fig. 1 is showing the 8T schematic which is followed by Fig. 2 i.e. layout of 8T circuit while drawing the layouts industry conventions are kept in mind i.e. metal layers 1,3,5 for horizontal connections and metal layers 2,4,6 for vertical connections [20], however only metal layers 1,2,3 are used as these layers have sufficiently met the task of making connections. Similarly Fig. 3 depicts 11T schematic and its corresponding layout is shown in Fig. 4. Fig. 5 and Fig. 6 are showing the schematic and layout of 12T optimized circuit respectively. There is a slight difference in the layout and schematic of 18T conventional D Flip Flop circuit, because the schematic and layout for 18T is designed by following the bottom-up approach i.e. the schematic is designed by instantiating the NAND instance and INVERTER instance designed separately in the tool, likewise the layout of 18T is designed by instantiating the layouts of NAND gate and INVERTER and assembling them to finally get the layout of 18T D Flip Flop. Fig. 7 and Fig. 8 are showing the schematic and layout of 18T D Flip Flop. The output waveforms of 8T and 12T are shown in the Fig. 9 and Fig. 10 respectively. The

reason to take waveforms of 8T and 12T is just to make a superficial observation of the working of two circuits. The waveforms for 11T and 18T are similar depending on the time period and pulse period of input signals.

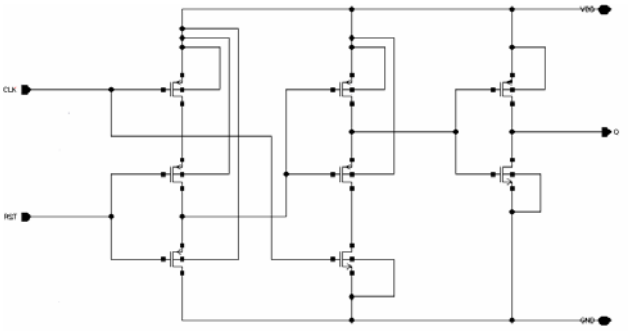


Fig.1. 8T Schematic

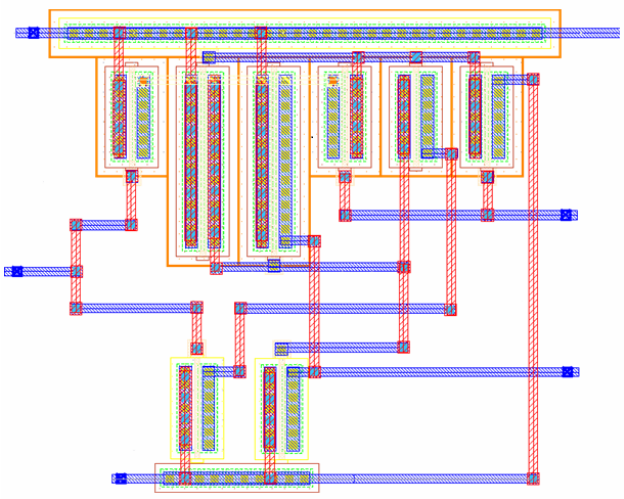


Fig.2. Layout of 8T D Flip-Flop

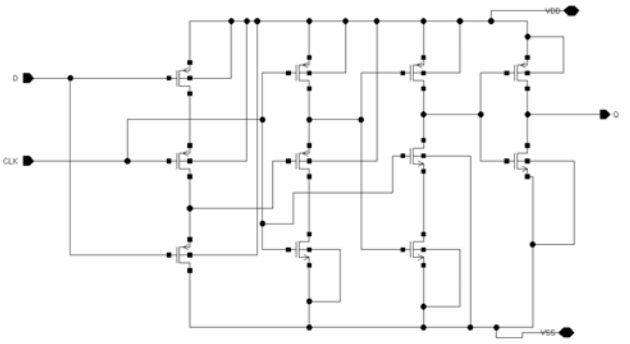


Fig.3. 11T Schematic

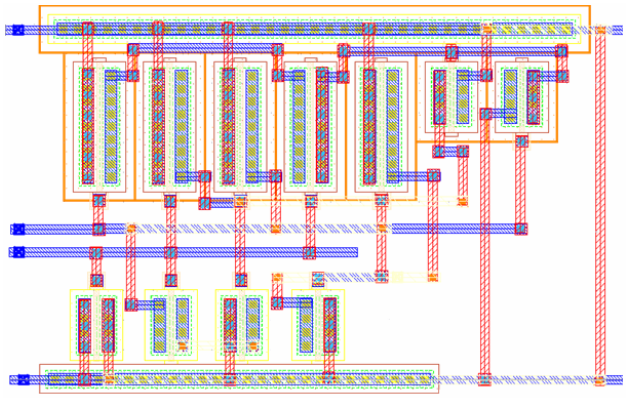


Fig.4. Layout of 11 Transistors D Flip-Flop

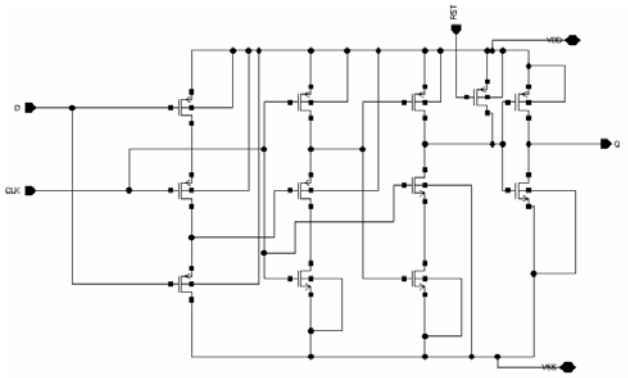


Fig.5. 12 T Schematic

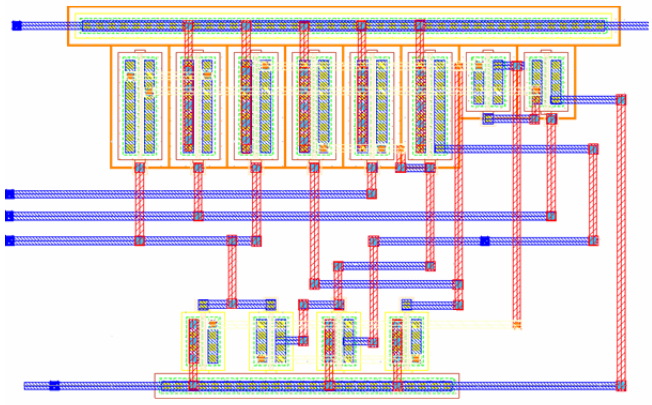


Fig .6. Layout of 12 Transistors D Flip-Flop

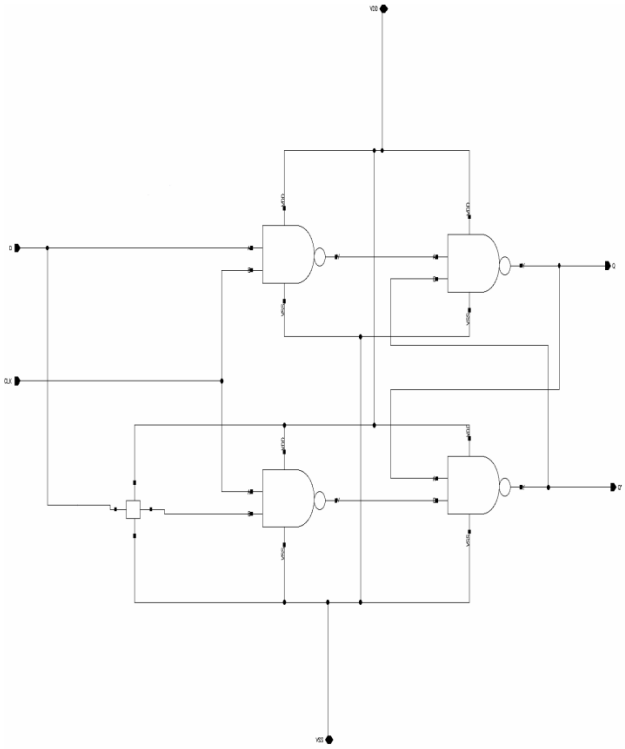


Fig.7. Bottom Up design for 18T D Flip Flop Schematic

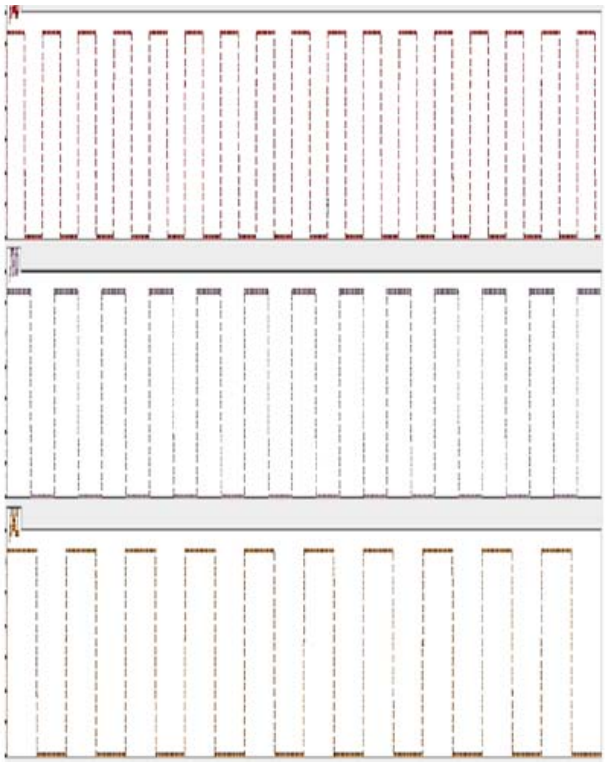


Fig.9. O/P Waveforms of 8T D Flip-Flop

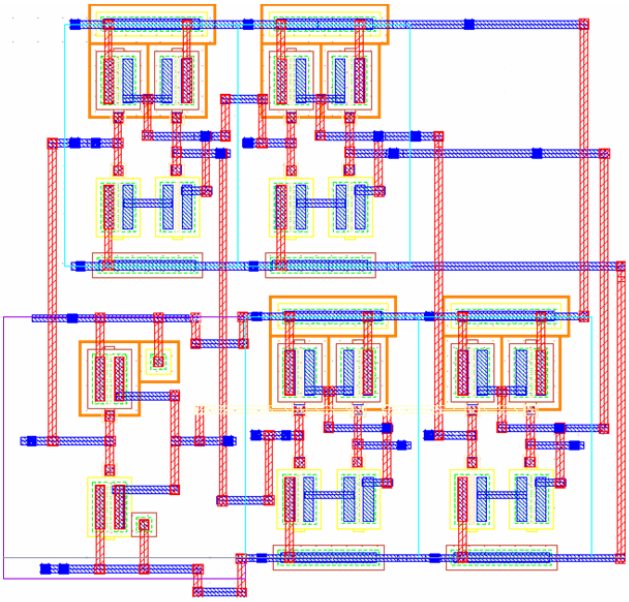


Fig.8. Layout of 18 Transistors D Flip-Flop

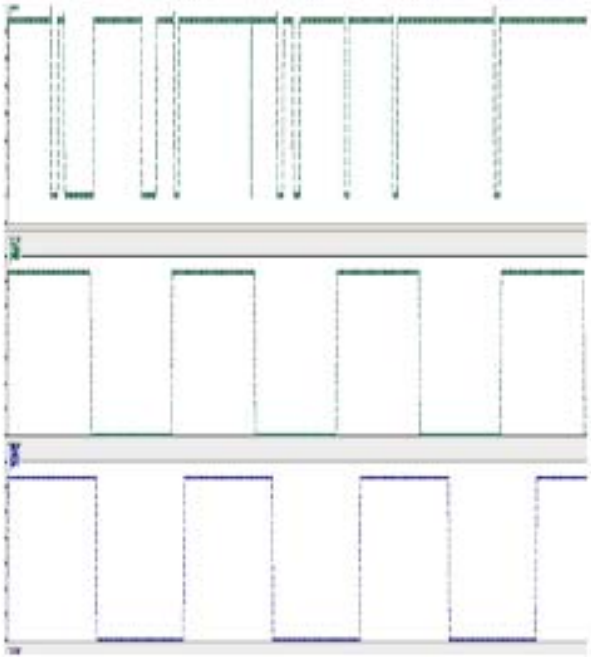


Fig.10. O/P Waveforms of 12T D Flip-Flop

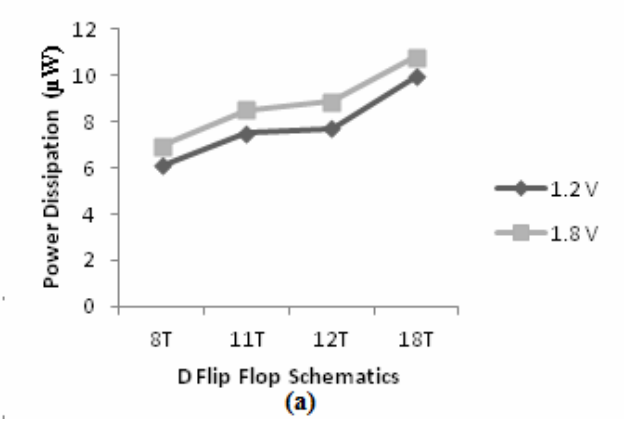
5. RESULTS AND DISCUSSION

The different circuits have been simulated in Cadence Virtuoso tool in 180 nm technology. The parameters and concerned results are shown in the Table-2. The results are calculated for two supply voltages i.e. 1.2V and 1.8V so that the effect of the supply voltage variation can also be adjudged [20]. It can be inferred from the table that logic optimization of the circuit is beneficial with respect to all the parameters of the comparison that is power dissipation, delay and leakage power. There observed a substantial reduction of 36% in power dissipation when the designs of 18T and 8T are compared for supply voltage of 1.8V. As far as delay is concerned 11% of reduction in delay is observed. In parallel 23% reduction in leakage power is noted. In Fig. 11 (a,b,c,d) plots depicting the nature of variation of power dissipation, delay, power delay product, and leakage power are shown.

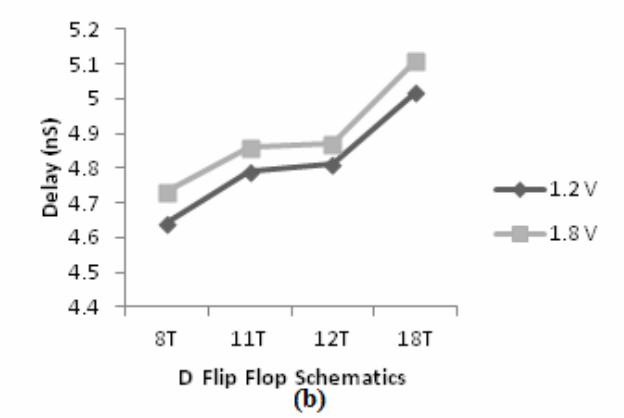
From plot (a), Fig. 11, it is clear that there is no much variation in the power dissipation value for 12T and 11T, but there is a steeper change in its value from that of 18T to that of 12T and from that of 11T to that of 8T. A similar trend is observed in the Delay parameter variation as can be seen in the plot (b), Fig. 11. However change in the parameter of delay is steepest from that of 18T to that of 12T, in other plots change is not that steeper. The power delay product variation is also showing the similar trend as can be seen in the plot (c), Fig. 11. Plot (d), Fig.11, is depicting the variation in leakage power for different designs, however it can be seen in the plot that variation remained almost linear and steepness of the curve is almost same in each portion of the graph, thereby indicating a gradual linear reduction in the leakage power from that of 18T to that of 8T.

Table 2 : Comparative Results of Different Circuits

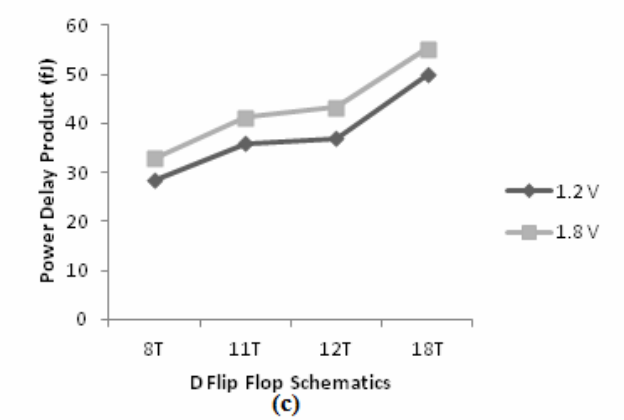
Parameters	8T		11T		12T		18T	
	1.2 V	1.8 V	1.2 V	1.8 V	1.2 V	1.8 V	1.2 V	1.8 V
Power Dissipation (µW)	6.12	6.95	7.51	8.49	7.69	8.89	9.96	10.81
Delay(nS)	4.64	4.73	4.79	4.86	4.81	4.87	5.02	5.11
Power Delay Product (fJ)	28.4	32.9	35.9	41.3	36.9	43.3	49.9	55.2
Leakage Power (nW)	378	395	422	451	428	454	465	489



(a)



(b)



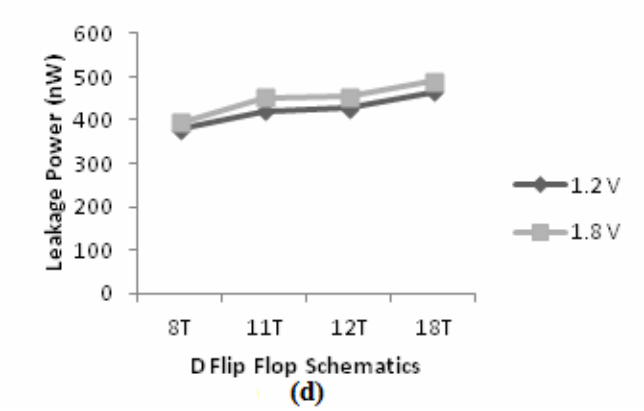


Fig. 11. D Flip of Flop vs Various Parametres (a) Power Dissipation (μW) (b) Delay (nS) (c) Power Delay Product (fJ) & (d) Leakage Power (nW)

6. CONCLUSIONS

It is concluded from the above study that 8T D flip flop is having lowest values for various parameters under study when compared with other optimized circuits. It is further noted that 8T design is the most optimal design among all the circuits.

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