Low Power CMOS Dynamic Latch Comparator using 0.18µm Technology

Rahul Singh*[1], and Arun Sharma[2]

ABSTRACT

The design and analysis of low power, high speed CMOS dynamic latch comparator is presented. The comparator combines the features of both, the resistive dividing network and differential current sensing comparator. The proposed design will improve the comparator performance by reducing the propagation delay, power dissipation. Simulation results are obtained in 0.18um with supply voltages of 1.8v respectively. The schematic of comparator is captured using Cadence Virtuoso schematic editor and simulated using the Cadence Spectre simulator.

***Key words** : ADC, Charge sharing network, latch comparator, charge sharing comparator, low power consumption.*

1. INTRODUCTION

A Comparator is a circuit that compares an analog signal with another analog signal or reference & outputs a binary signal based on comparison. The comparator is widely used in process of converting analog signals into digital signals. Low power consumption is an important feature of many A to D converters especially those used in portable devices that have limited power supply energy. A common technique to reduce its power is the adoption of a latch comparator design. Dynamic latch comparator can solve the power problem by removing the pre-amplifying stage [1], while achieving a smaller area. This paper focuses on charge sharing comparator as it combines the advantages of both, resistive dividing comparator & differential current sensing comparator.

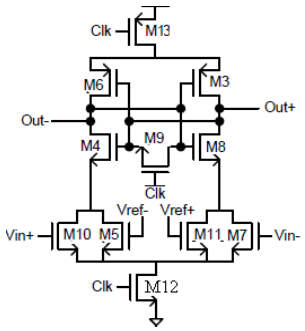

Fig. 1. CMOS charge sharing topology for dynamic latch comparator[4].

Fig.1 shows the charge sharing topology for dynamic latch comparator [4]. In the fig.1, nMOS transistor M12 is used in series with resistive comparing circuit for regenerative mode in order to achieve low power. For reset mode pMOS pre charging circuit is absent and nMOS transistor M9 for output pass transistor for the equalization of both the voltages nearly to Vdd/ 2. Now, when the clock goes low, Vdd and ground both will be disconnected from the latch with the help of transistors M12 & M3.

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2. DESIGN OF THE COMPARATOR

The flow chart shows in Fig. 1 shows the step of designing the low power CMOS charge sharing dynamic latch comparator using 0.18ìm technology:

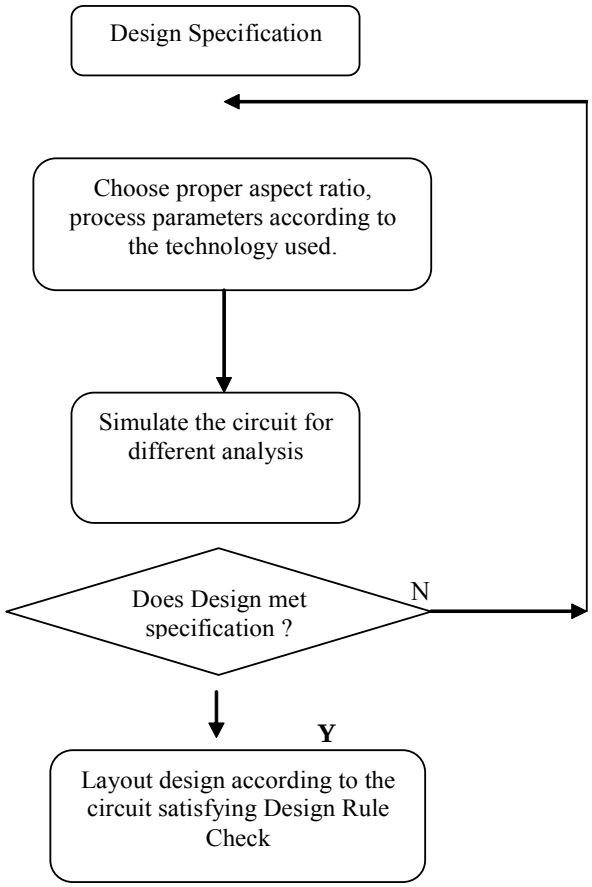

Fig. 2. Flow chart for designing of comparator

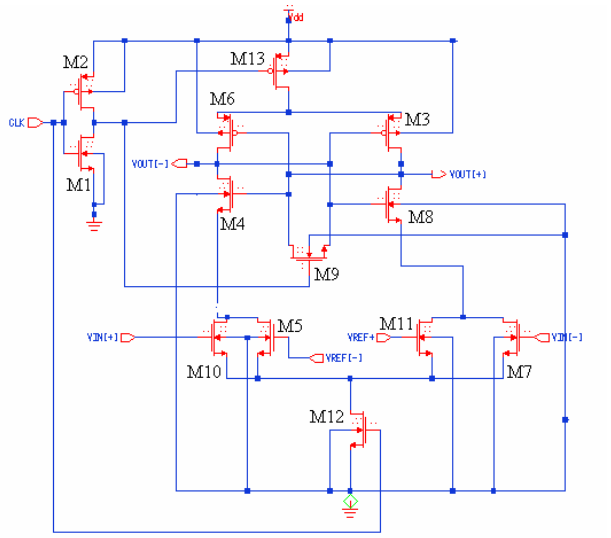

Fig. 3. Design of comparator

Fig. 3 shows the simulated output voltage waveform of this circuit when Vref+ = Vref- = 0.9V and Vin+ = Vin- = 1.8V is a square wave. The parameters of all the transistors are shows in Table I.

Table-I
CMOS Transistor Parameter

	All PMOS	All NMOS
Width	8µm	4µm
Length	0.18µm	0.18µm

If the input of the comparator is greater than the reference voltage, Vref, it has to give an output of '1' and if the comparator input is less than reference voltage then the output of the comparator should be '0'.

3. SIMULATION RESULTS

Simulation of proposed design is done using the 0.18ìm CMOS technology. In this project, 1.8V supply voltage is used for operation and clock period is 10ns. During the process, speed of the comparator is 100MHz. This design can be used where low power, high speed and low propagation delay are the main requirements. Finally simulation results of the comparator are shows in Fig. 4. The width of the transistor used is as in the Table I. This simulation result is compared to the previous work [2]. Table III shows the comparison of present design results with previous work and shows an improvement in the present results.

S-JPSET : ISSN : 2229-7111, Vol. 3, Issue 2

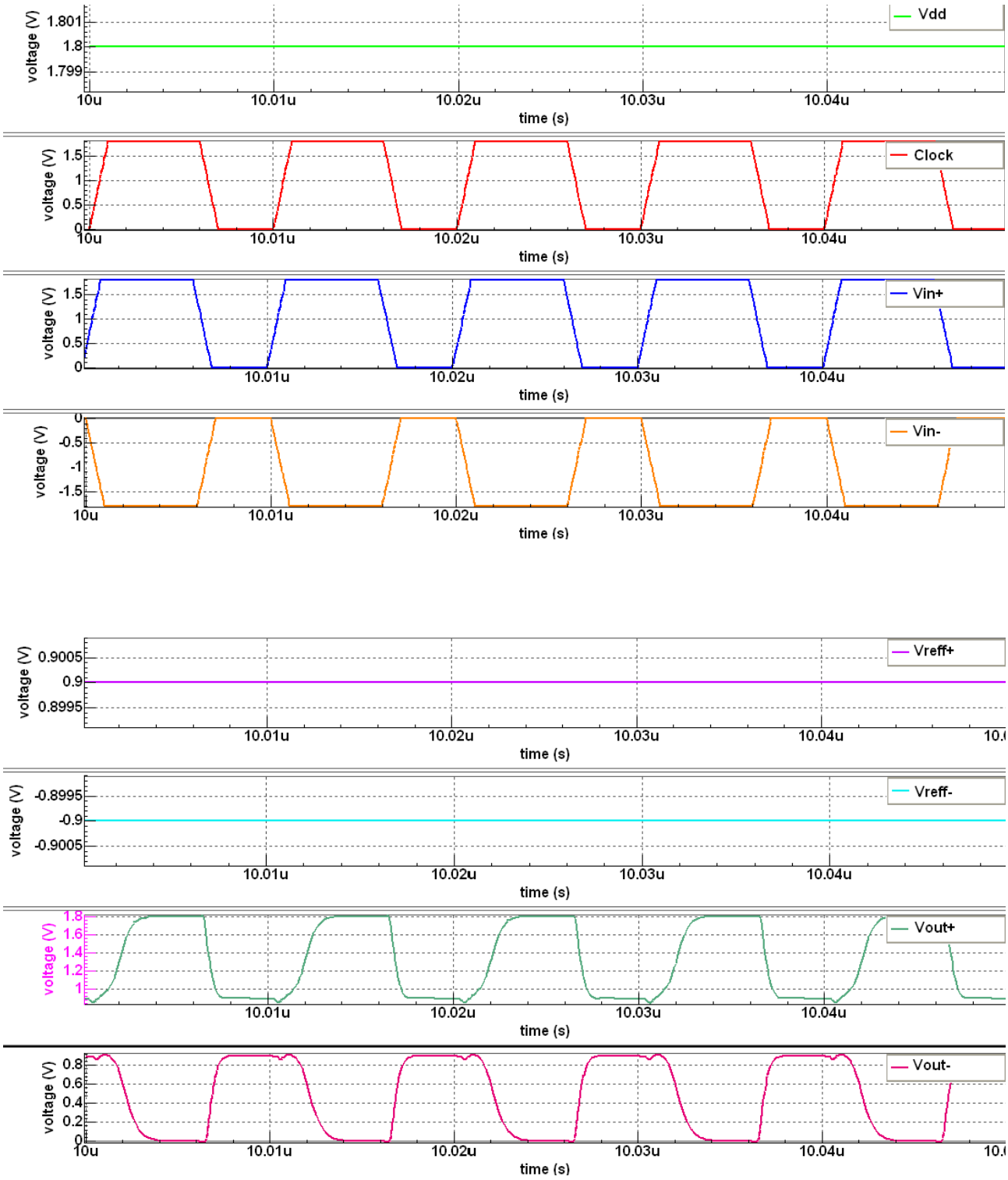

Fig. 4. Transient response

4. CONCLUSION

This paper has presented the CMOS charge sharing dynamic latch comparator design and its simulation results of high speed, and low power by considering 1.8V power supply. The comparison has been done between the previous and present work and the improvements are shown in Table II. In conclusion, the proposed design reduces the power dissipation without deteriorating the comparing speed. From simulation result the power dissipation reduced approximately 92% compared to the previous work and minimize the delay approximately 15%. The proposed design of the comparator runs faster and provides more stable output signal than the previous work with low supply voltage.

Table-II

	Previous work	Present work
Length	0.5µm	0.18µm
W_p / W_n	10µm/5µm	8µm/4µm
Voltage supply	3.3V	1.8V
Delay	1.827ns	1.54ns
Power dissipation	23.18nW	1.79nW

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