Study and Performance Analysis of MOS Technology and Nanocomputing QCA

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Abstract

One of the critical issues in VLSI circuit is High Power dissipation. Quantum-dot Cellular Automata (QCA) which is widely utilized in nanocomputing era. QCA has Landauer clocked based synthesis approach and it has clocked based information flow. This manuscript analysis and design a combinational digital circuits in an emerging QCA framework. The design is evaluated and formulated in terms of area, latency and power dissipation. QCA Designer tool has been taken for the design of quantum cell-based combinational circuits and simulation purpose. Moreover, it is believed based on experimental analysis that the QCA based combination circuits will make a contribution to high computing speed and low power paradigm.

1. INTRODUCTION

Nanotechnology has been an advanced domain that broadens the perspective of nanocomputing device in the recent years. Conventional CMOS has a challenge for optimizing the power dissipation in computing systems. In nanotechnology, the power as well as area has been optimizing. New nanotechnology alternatives such as carbon nanotube, resonant tunnelling diodes, spintronic etc. that can tackle the problem existing in conventional CMOS based circuit design [1]. In the approach, quantum-dot cellular automata (QCA) are the suitable technology, which has solved the problem of CMOS transistor [2]. In QCA technology, a cell bounds two free electron and the logic binary value 1 and 0 depends on the position of an electron inside the quantum-dot cell, which is driven by columbic interaction.

This paper introduces a new design for a QCA multiplexer in which the majority and inverter gate is utilized and simulated in QCADesigner using a coupling of quantum cells. A new 2:1 multiplexer based on a coplanar technique in QCA with using a less number of cells and area. Optimized design is introduced in which the cell count, size and latency are optimized to improve efficiency.

The rest of the manuscript is organized as follow: an introduction to QCA preliminaries and a review of QCA multiplexer structures are provided in section 2 and section 3, respectively. The construction of QCA multiplexer is addressed in section 4. The simulation results in discussion over the proposed combinational multiplexer and its performance evaluation are presented in section 5. Finally, section 6 concludes this work.

2. PRELIMINARIES

The simple QCA unit is a cell that contains 4 quantum-dots located at the corner of a quadrangle. In each cell, 2 electrons can be located only in the diametric corner in accordance with Coulomb electrostatic interaction [4]. These electrons are controlled by potential barriers and could be displaced by tunnelling potential, control of the potential barriers, or creation of binary values. It

is assumed that tunnelling out of the cell is not possible because of the existence of large potential barriers. In the molecular scale QCA, the electronic charge was introduced to save and flow of the data [5]. The binary information can be encoded as -1 and 1 polarities for binary '0' and '1', respectively, to create the digital logic bits in the QCA design (Shown in Figure 1a). If two cells are adjacent, the Coulomb interaction between the electrons causes the cells to have equal polarization and equal portions of the left-side cell [6]. The basic digital logic unit in the QCA is the majority gate and inverter (Shown in Figure 1b, 1d). The logic equation for a majority gate is expressed as M(A, B,C) = AB + AC + BC.

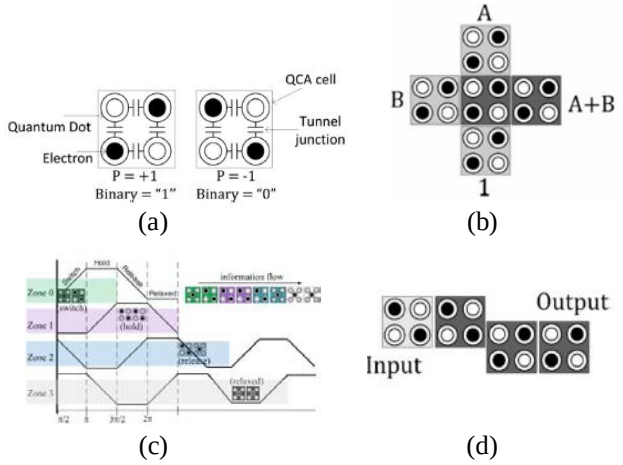

Fig.1: QCA basic (a) Quantum cell (b) Majority gate (c) Clocking (d) Inverter

Setting the appropriate polarization of one majority gate input constant at 1 or 0 design either an OR or AND logic gate, respectively. Another useful logic gate in the QCA is the inverter gate (Shown in Figure 1d). Using the AND, OR and NOT gates, any digital logic circuits can be constructed and designed. QCA clocking mechanism is shown in Figure 1c.

QCADesigner tool is used to simulate the QCA designs. Normal cells (in four zones), rotate cells, fix polarization cells and input/output cells are used in the design.

3. COMBINATION LOGIC DESIGN IN CONVENTIONAL CMOS

In this section, we have designed the various combination logic gates such as NAND and NOR in conventional CMOS technology. Simulations on the extracted layouts of these logic gates discussed in this paper are performed using Micro wind EDA tool. To check the worst power consumption of CMOS NAND, and CMOS NOR, using the exhaustive test vector is shown in Fig. 4. A two transistor PMOS and NMOS is taken for the construction of CMOS NAND and CMOS NOR design, shown in Fig. 2a, 3a. The simulation result of CMOS NAND and CMOS NOR is presented in Figure 2b, 2c.

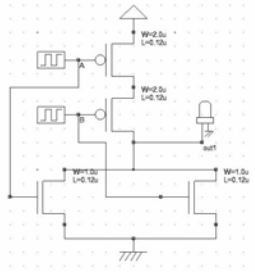

Fig.2a : Circuit realization of CMOS NOR

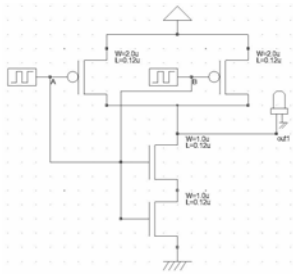

Fig.3a: Circuit realization of CMOS NAND

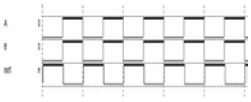

Fig.2b: Simulation waveform of CMOS NOR

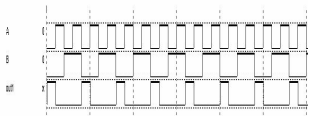

Fig.3b: Simulation waveform of CMOS NAND gate.

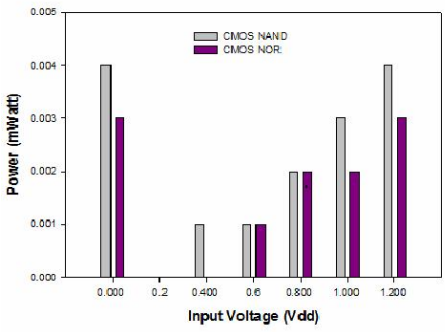

Fig.4: Power versus Supply voltage

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gate.

This design faces fundamental problems in terms of power dissipation and footprint area. But in order to enhance the overall performance of the design, research is carried out to find and alternative to transistor-less technology such as QCA. QCA is one of the promising technologies that provide unique features such as high speed, and low power.

4. COMBINATION LOGIC DESIGN OF MULTIPLEXER IN QCA

The proposed design can be used to construct some circuits such as a 2-to-1 multiplexer. The logical function of a 2-to-1 multiplexer as $\overline{\text{Sel}}A + \text{Sel}B$. New combinational 2:1 QCA multiplexer design is shown in Figure 5a. This design utilizes of 32 cells covering an area of 0.034 μm^2. The new QCA type multiplexer has been designed and simulated using the popular QCADesigner tool.

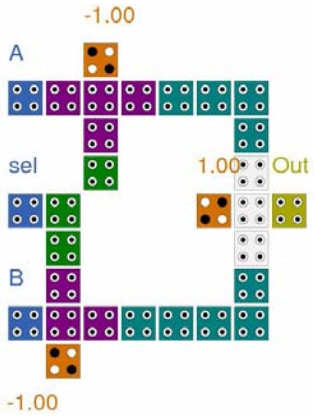

Fig.5a The layout of 2-to-1 multiplexer based on QCA

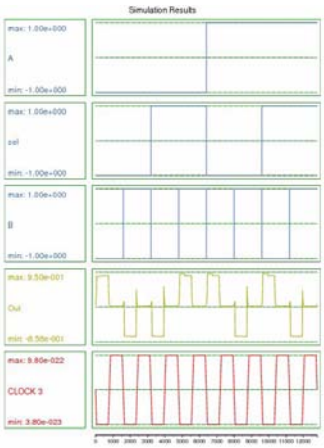

Fig.5b Simulation result of 2:1 multiplexer

5. SIMULATION RESULTS

In this section, validation of the functionality of the new designs is carried out by leveraging QCADesigner tool. Although only the default parameters for the Bistable engine are taken, for simulation. Bistable Approximation, yield same outcomes. The simulation results of a 2-input multiplexer with one select line that is constructed using quantum cell are illustrated in Fig. 5a. The 2:1 multiplexer simulation results along with the input and output waveforms are provided in Fig.5b.

6. COMPARISION RESULTS

Different QCA gates can be designed using the construction of 2:1 multiplexer. It is inferable from comparative analysis result that the new multiplexer has surpassing significant improvements in QCA circuits. Comparison results between the new multiplexer and the existing multiplexer in terms of cell count and area indicate that the new design of multiplexer in comparison to this design leads to significant improvement in terms of complexity and area. Based on these results, the new layout can be used as a suitable component for designing larger robust QCA circuits. The area and complexity of new multiplexer and existing design can be seen in Table 1.

Table-1 : Comparative Analysis

2:1 Mux	Cell count	Area (μm^2)
[4]	88	0.14
[5]	46	0.08
New	32	0.34

7. CONCLUSION

The multiplexer is a basic and popular unit in ALU and processor unit. This article presents a new and area efficient design of 2:1 multiplexer in QCA. The proposed multiplexer unit, which is

structured by coplanar technique and, have been simulated using QCADesigner tool and tested in terms of cell count, area and latency. As it was, apparent in simulation results, the proposed multiplexer has superiority over the existing designs in QCA and the comparisons evidently showed significant improvements.

REFERENCES

[1]. C.S.Lent, P.D.Tougaw, W.Porod, and G.H.Bernstein, "Quantum cellular automata," Nanotechnology, vol.4, no.1, pp.49–57, 1993.

[2]. W. Porod, "Quantum-dot devices and quantum-dot cellular automata", Inter. J. Bifurcation and Chaos, vol. 7, no. 10, pp. 2199-2218, 1997.

[3]. Tougaw, P. Douglas; Lent, Craig S.; , "Logical devices implemented using quantum cellular automata," Journal of Applied Physics , vol.75, no.3, pp.1818-1825, Feb 1994.

[4]. Kim, K., Wu, K. and Karri, R., 2007. The robust QCA adder designs using composable QCA building blocks. IEEE transactions on computer-aided design of integrated circuits and systems, 26(1), pp.176-183.

[5]. Teodosio, T.; Sousa, L.; , "QCA-LG: A tool for the automatic layout generation of QCA combinational circuits," Norchip, 2007 , vol., no., pp.1-5, 19-20 Nov. 2007

[6]. N.K. Misra., S. Wairya, and V.K. Singh, "Approach to design a high performance fault-tolerant reversible ALU". International Journal of Circuits and Architecture Design, Inderscience, 2(1), pp.83-103, 2016.

