

Low Power Differential & Ring Voltage Controlled Oscillator Architectures for High Frequency (L-Band) Phase Lock Loop Applications in 0.35 μ Complementary Metal Oxide Semi Conductor Process

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Abstract

The design of a high frequency (L Band), low power (2.75mW) Phase Lock Loops with a 350nm Complementary Metal Oxide Semi Conductor (CMOS) technology has been represented. The comparison of Current Starved Voltage Controlled Oscillator (CSVCO) and Differential pair VCO is performed and analyzed for low power and high frequency analysis respectively. Each component of Phase Lock Loop (PLL) is designed with 350nm CMOS technology in Design Architect Integrated Circuit Station by Mentor Graphics (Eldo-Net) as simulator. In this paper both the standard configurations have been simulated under the same environment and results are analyzed for two most important Very Large Scale Integration (VLSI) constraints, Speed (High frequency range) and Power consumption. The high speed and locking performance of the Differential pair VCO has been evaluated against the lower power consumption benefit of CSVCO.

1. INTRODUCTION

The phase sensitive detection of closed loop frequency controlled functioning depends upon phase difference between the input and output signals of the control block. Voltage Controlled Oscillator (VCO) integrated in the phase-locked loops (PLL) is the integral part of the frequency synthesizers and clock recovery circuits. PLL circuits are now frequently used to demodulate FM signals making obsolete the Foster-Seeley and radio detectors of the early years. A Voltage Controlled Oscillator finds variety of applications and therefore results in different architectural designs such as LC oscillator, Resonator circuit (using Ring architecture), Relaxation Oscillator etc. Due to better speed and higher stability in

output oscillations, the differential amplifier based ring oscillator is used with less number of stages which results in reduced power consumption [1]. This crucial aspect of the differential amplifier configuration has inspired this work to remain focused around it. Further lower power consumption can be obtained using some other configurations such as Partial Positive Feedback system and Ring Oscillator architecture [2]. LC tuned circuit based oscillators have proved their supremacy for the high frequency (microwave band) applications, but the advantage costs in terms of circuit complexity due to designing of inductors [3]; whereas a ring architecture has an added advantage of smaller area as compared to the LC oscillator. Ring oscillator shows an added advantage of wide tuning range also [4].

Since past many researches and publications came in focus whose realization differ in their frequency of operation, tuning range, phase noise characteristics, power consumption, circuit architecture and level of integration. Plenty of researches have been conducted in realizing a high lock range PLL with lesser lock time and power [5-6]. There were papers on Mixed Signal Analysis and Low power design using technologies ranging from 600 nm to 22 nm [7].

In this work, the design specification for 350nm technology has been chosen for having lesser high order effects and achieving higher Signal-to-Noise (S/N) ratio. The paper describes the design of 1.8GHz, 2.75mW PLL that has been simulated with 0.35- μ m CMOS technology in IC-Station (Mentor Graphics) on Eldo-Net simulator. Evolving from single stage oscillator, the PLL employs various circuit techniques to achieve high tunable frequency range with low power dissipation.

The main aim of the paper is to design and perform the comparative analysis on two different VCO design aspect that are Current Starved VCO (CSVCO) and Differential Pair VCO (DAVCO) on the basis of tunable frequency range (speed), power dissipation, tracking range and performance.

2. VARIOUS STRATEGIES FORMATION FOR PLL

The standard architecture of PLL (shown in fig. 1) is a fairly standard topology. It consists of Phase Detector (PD) that generates an output signal which is proportional to the difference between the reference signal and the divided down signal, Charge pump and Loop Filter to receive digital pulses and convert them into an analog control voltage V_{control} , and a voltage-controlled oscillator (VCO) with the purpose of either speed up or speed down the feedback signal according to the error generated by PFD[8].

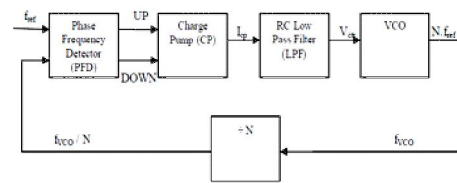


Fig.1: Phase-Locked Loop architecture

Instead of using the most basic phase detector which is simply an Exclusive-OR gate, Phase Frequency Detector (PFD) has been employed here. It has been designed from D flip-flop which in turn is designed by using 2I/P and 3I/P NAND gates to eliminate the problem of locking onto harmonics of reference signal. Charge pump with bootstrap buffer is incorporated in the design to overcome the issues of Charge Sharing, Mismatch between Drain Currents and Delay differences.

The design of PLL has evolved from a one-stage ring oscillator, and is described in a progression starting from the VCO circuit. This paper compares the design methodology, schematic complexities and performance of the two prescribed VCO's, CSVCO and Differential Pair VCO. The selection of the VCO depends upon the requirement of high tunable frequency range or low power design. The range of frequency of the PLL is concentrated by properly choosing the circuit architecture and parameters.

3. ARCHITECTURE PROPOSAL FOR VCO

A Voltage-controlled oscillator (VCO) is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. The most commonly used architecture for VCO in CMOS technology is voltage controlled ring type oscillator. It consists of several delay cells forming a closed loop. The study of previous researches post some challenges in the VCO design that is achieving high frequency to get wide tuning range, getting constant output swing (linearity) and stability of the design [9]. The paper proposes the

following two VCO designs that can be used according to the requirement.

3.1 Current Starved Voltage Controlled Oscillator (CSVCO)

The schematic view of the CSVCO has been shown in fig. 2. Its operation is very much similar to Ring oscillator. MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources M1 and M4 limit the current available to the inverter M2 and M3. In other words, the inverter is starved for current. The drain currents of MOSFETs M5 and M6 are the same and are set by the input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage.

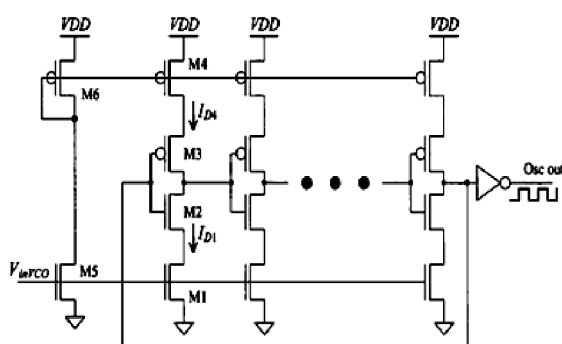


Fig.2: Current Starved VCO

3.2 Differential pair VCO

Ring oscillators have been widely used as VCO's in phase locked systems [5]–[7]. Providing a wide tuning range with relatively constant voltage swings, these oscillators also lend themselves to low voltage operation. Differential VCO is also a ring type oscillator as shown in the basic block diagram in fig. 3.

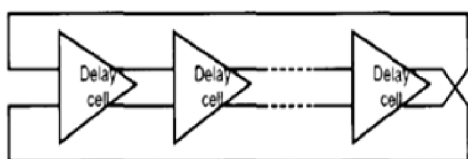


Fig.3: Ring type oscillator

The Differential VCO is designed to achieve high frequency range. The first step in designing the VCO was to design a delay cell. A delay cell consists of a basic differential operational amplifier. The two PMOS transistors in this delay cell were designed to operate in the linear region so as to act as variable resistors. This is necessary in order to control the output frequency by varying the resistance. This is because the frequency depends on the time constant of each delay cell which is varied by changing the resistance[10]. The remaining PMOS transistors were sized to operate in the saturation region. Here PMOS is driving circuit so we are using NMOS as active load. Fig. 4 shows the schematic of a delay cell.

This type of delay cell has a major drawback as it cannot maintain a constant output swing. This occurs because as $V_{control}$ changes, V_{out+} and V_{out-} will also change. This occurs because as $V_{control}$ changes, the resistance across the PMOS transistors always changes. A change in those points causes the output swing to vary and thus introduces nonlinearity. The solution to this drawback was to create a control circuit. The main aim is to provide biasing current from internal circuitry rather than different biasing circuit for each stage[11-12]. This makes design simpler. V_{b1} and V_{b2} from the control circuit control the current in each stage of the differential oscillator. Hence it controls the delay of each stage and therefore the oscillation frequency increases or decreases according to the variation in the delay of each stage.

The $V_{control}$ is given at the lower part of the control stage circuit and to the active load of each ring differential stage. More number of stage result in lowering frequency range as frequency is inversely proportional to two times delay of all stages and the low number in stage is unstable. From the view point of speed-power trade off

[13-14], it is desirable to decrease the number of stages in a ring to the extent possible, so in these design, seven stages of ring differential pair is used. Fig. 5 shows the schematic of Differential VCO where the control voltage can be seen before the differential stage which is used for biasing all the seven stages.

The output clock frequency is determined by the delay of each delay cell which in turn is controlled by control voltage. A wide frequency range of oscillator means a wide tuning range of each delay cell. The delay cell is usually a differential pair with a tail current and some active loading. The delay of each cell is controlled by the tail current.

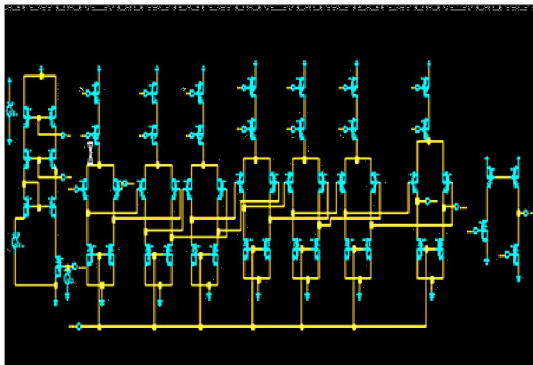


Fig.4: Proposed schematic design of differential pairing VCO

There are some difficulties associated with this architecture in order to achieve the wide tuning range. By using a single tail current, the tuning range is limited by the control voltage range. The control voltage is usually constraint by the power supply voltage, i.e. $0 \leq V_{\text{control}} \leq V_{\text{dd}}$, where V_{dd} is the supply voltage, a constraint associated with the design technology. If we choose the small tail current, the tail current is still not large enough even that the control voltage reach the up limit so that the high end frequency range of VCO is small. On the other hand, if we choose the large tail current, the tail current is still large even that the control voltage reached the lower limit so that the lower end frequency range of VCO is large [8].

4. DESIGN PERFORMANCE & SIMULATION RESULTS

The design of PLL that was chosen here was Digital PLL which incorporated both analog and digital counterparts. The digital part was PFD and divider network. The PFD was analyzed to detect both phase and frequency and using 2 and 3 input NAND gates; the problem of locking onto harmonics was eliminated. With the improved Charge pump design, the work has been successful in obtaining stable and high frequency outputs with a very low phase noise. Also the power was significantly reduced by proper sizing of Divider network transistors and employing it in Master Slave pattern. Both the VCO's that were discussed in previous section were designed separately and employed in the design of PLL at the place of oscillator block. For the VCO's, performance characteristics and comparison of PLL is drawn.

With lesser complexity and lesser number of stages in the oscillator design, the Current Starved VCO results into the low power consumption design where as with total Seven stages in the differential pair VCO along with the control stage employed for internal biasing results in complex and comparatively high power consuming design, although both the designs succeeded in achieving wide tunable frequency range. Differential pair VCO operates at higher range of frequency where as Current Starved VCO operates at comparatively lower frequency range. From the simulation results, the Differential pair VCO shows high frequency gains near to 900MHz/V where as the Current Starved VCO is limited in mid 50's MHz/V. The proposed design has succeeded in achieving small settling time and locking time. This show that the proposed PLL design acquires locking stage very fast in comparison to other PLLs thus can be called as fast acquisition Digital PLL.

Both the proposed designs have been implemented and simulated under the common simulation platform. The comparative results have been discussed under following major concerns:

- High speed (frequency of Operation)
- Low power dissipation
- Linear response (frequency vs Vcontrol)
- Locking time

4.1 Output Frequency and Linearity

One of the most important aspects of VCO design that is the output oscillation's linearity with respect to the input tuning voltage (Vcontrol) has been plotted in fig. 5 and fig. 6.

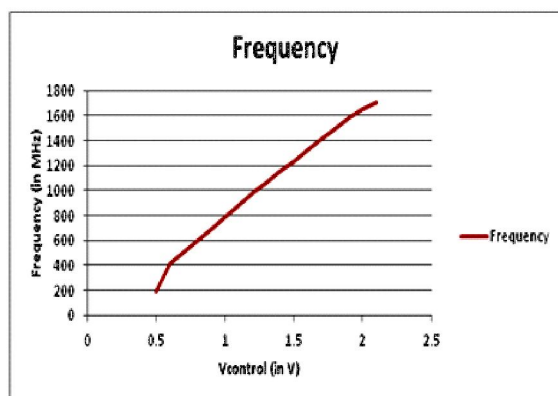


Fig.5: Differential VCO characteristic curve

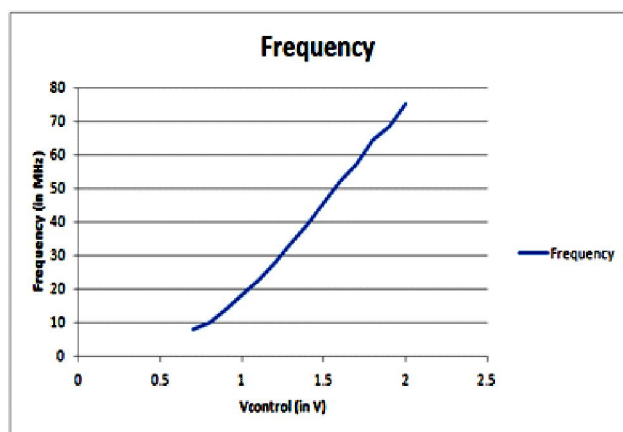


Fig.6: Current Starved VCO characteristic curve

Here one can observe for the Differential VCO PLL that the linear range is far more extended in GHz than the Current Starved structure. A significant

difference in highest frequency operation and fairly larger linear range of differential amplifier must be appreciated.

4.2 Power Consumption by PLL architecture

Table: 1 shows the amount of power consumed by various component of Differential VCO PLL (DA-VCO). Fig. 7 explains the same in pie-chart diagram format, for the Current Starved VCO PLL (CS-VCO).

Table-1: Power Consumed in Differential VCO PLL

Component	Power Consumed (mW)
VCO	49.21
PFD	0.3
CHARGE PUMP	4.2
FREQUENCY DIVIDER	0.25

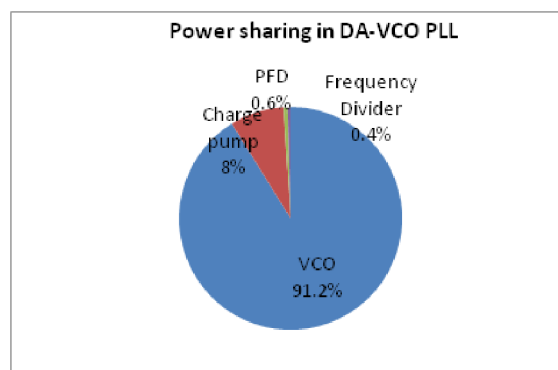


Fig.7: Power Consumed in Differential VCO PLL

For DA-VCO PLL, VCO itself consumes the maximum power of 91% of the total PLL design. The lowest power is consumed by frequency divider. It only consumes about 0.4% of total power. Charge pump consume 8% power while PFD consume 0.6% of the total power (Fig. 7).

Table 2 shows the amount of power consumed by various component of Current Starved PLL, where VCO consumes maximum power of 58%. The lowest power is consumed by frequency divider again which is about 9% of total power. Charge pump consume 22% power while PFD consume 11% power

Table-2: Power consumed in Current Starved VCO PLL

Component	Power Consumed (mW)
VCO	1.54
PFD	0.3
CHARGE PUMP	0.58
FREQUENCY DIVIDER	0.25

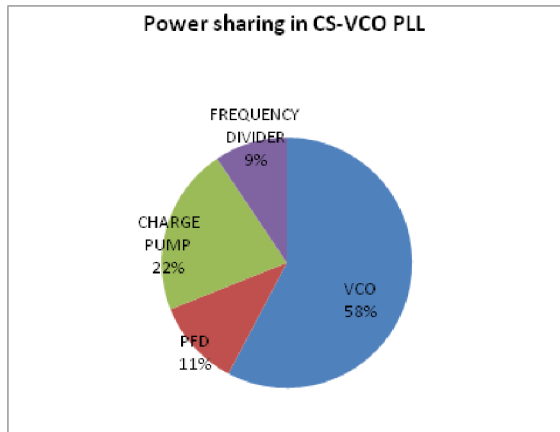


Fig.8: : Power consumed in Differential VCO PLL

The power consumption of Differential pair VCO and PLL is much higher than PLL using Current starved VCO due to large number of transistor used. In this design VCO consume about 91% of total power while power consumed by frequency divider is almost negligible. Charge pump consume 8% of total power while PFD 1% as shown in fig. 8.

Thus total power consumption of Differential Amplifier PLL is about 54.91 mW, whereas only 2.67 mW by Current Starved PLL. This result clearly appreciates the lowest power consumption property of CMOS inverter design for Current Starved VCO.

5. CONCLUSION

The paper discusses the comparison and implementation of two designs of VCOs. Current starved ring oscillator has been considered for its superior performance in form of its low power consumption and wide tunable frequency range and Differential pair VCO is considered for its high frequency and wide tunable frequency. It has been

analyzed that the designed PLL using current starved VCO consumes 2.75 mW power from 1.3 V supply and have a smaller lock time. PLL using differential VCO consume 54.91 mw. The curve of differential VCO is linear in range of 400 MHz and 1.72MHz. So the centre frequency is about 1 GHz and wide tunable range is achieved using it.

Therefore, for the speed and linearity concern, Differential architecture for VCO proves to be a better choice, especially for the fast communication devices, whereas the demanding need of lower power consumption for the remote wireless circuits still finds the Current starved VCO as a more prominent configuration. With the improved Charge pump design, one is able to obtain stable and high frequency outputs with a very low phase noise. Also the power could be significantly reduced by proper sizing of Divider network transistors and employing it in Master Slave pattern.

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