RESEARCH ARTICLE

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Performance Analysis of Various Complementary Metal-oxide Semiconductor Logics for High Speed Very Large Scale Integration Circuits

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Abstract

The demand for VLSI low voltage high-performance low power systems are increasing significantly. Today's device applications necessitate a system that consumes little power and conserves performance. Recent battery-powered low-voltage devices optimize power and high-speed constraints. Aside from that, there is a design constraint with burst-mode type integrated circuits for small devices to scale down. Low voltage low power static CMOS logic integrated circuits operate at a slower rate and cannot be used in high performance circuits. As a result, dynamic CMOS logic is used in integrated circuits because it requires fewer transistors, has lower parasitic capacitance, is faster, and enables pipelined system architecture with glitch-free circuits. It has, however, increased power dissipation. Both types of CMOS circuits with low power dissipation overcome their own shortcomings.

This paper discusses dynamic CMOS logic circuits and their structures. Various logics are also discussed and on the basis of the results obtained, logic which is best suited for designing CMOS logic circuit will be found out. The logic on the basis of structure layout and design which gives best results for high-speed VLSI circuits, is found out.

Keywords: CMOS, Logics, Pre charge, VLSI.

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Introduction

Dynamic CMOS logic

A pre charge and evaluate logic circuit is a dynamic CMOS circuit logic. The main advantage of dynamic logic is that it requires fewer transistors, which makes it more useful. The pull down network of dynamic logic design with an n- transistor structure, whose output load capacitor is precharged to supply voltage by a pull-up p- transistor and discharged to the ground supply as per the input note condition by an n-transistor.

The enable signal for precharge and evaluate logic is the synchronies single-phase clock signal. The low signal at clock activates the precharge phase, while the high signal at clock activates the evaluation phase. Dynamic CMOS logic has the same input capacitance as pseudo-NMOS logic. The pull up p-transistor precharge[1] logicimproves the rise time of the output load, while the discharge ground switch improves the fall time.

Figure 1 shows the schematic circuit implemented using dynamic logic. In this a NAND logic is

design by series connected NMOS with precharge PMOS and evaluate NMOS transistors. The CMOSlayout structure is design in Figure 2.

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Although dynamic logic is designed with fewer transistors, some significant issues arise in this structure. The output node is always charged duringthe precharge phase is main issue .and it should be stable during the evaluation phase. A violation of the condition may result in charge redistribution, which may cause the output node to be falsely triggered. The second issue arises when dynamic logic is serially connected when multiple stages are required in design.

In this case, the output node of the first stage dynamic logic is connected to the input node of the subsequent stage dynamic logic. The output node of the first stage keeps the pull down transistor of the second stage in saturation

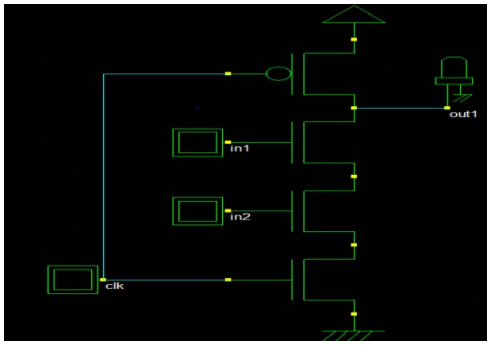

Figure 1: Schematic structure of Dynamic CMOS Logic

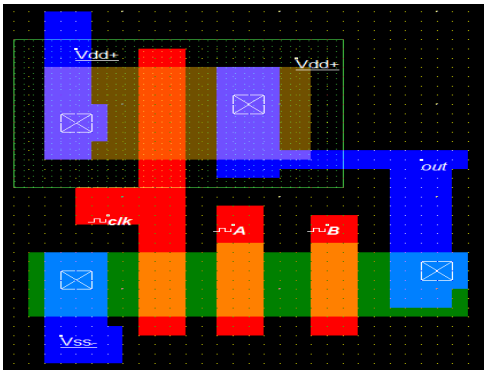

Figure 2: Layout of Dynamic CMOS logic

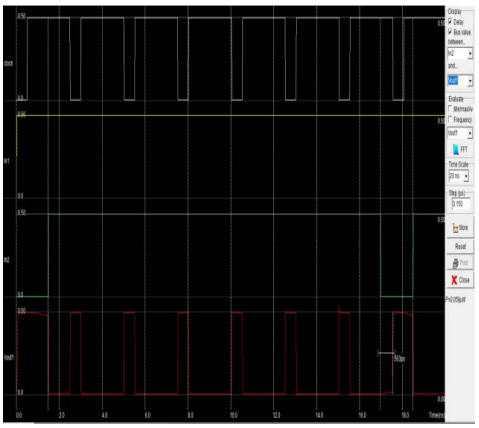

Figure 3: Timing Simulation of Dynamic CMOS logic

mode due to the finite fall time. Figure 3 depicts the timing simulation of dynamic logic.

The design layout consists of channel length of 0.075 µm, channel width 0.125 µm, rise delay 0.003 ns, fall delay 0.002 ns and power dissipation of 0.059 µW.

Cascade Dynamic CMOS

Cascaded single phase dynamic CMOS logic gates are not possible. The output level of one stage is used as an input to the second stage in series connected dynamic logic. Thus, during the precharge stage, both stages' output nodes are pre
charged to logic high. During the evaluation phase, the discharge voltage level of the principal stage conditionally

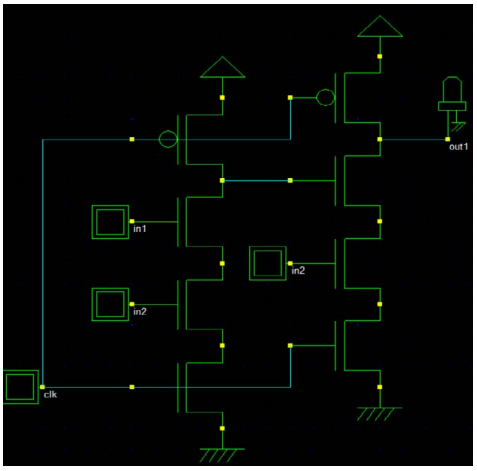

Figure 4: Timing Simulation of Cascade CMOS Logic

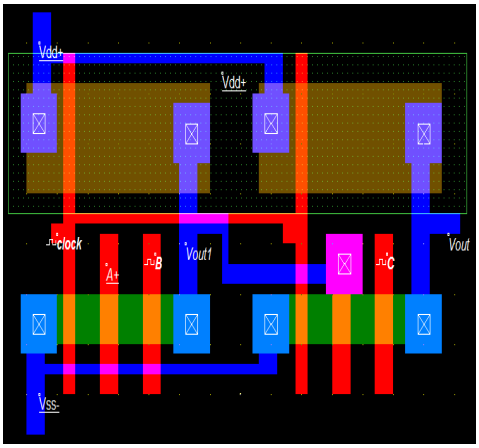

Figure 5: Layout of Cascade Dynamic CMOS logic

drives the input node of the second stage. This will be delayed due to the limited fall time. This delay will incorrectly cause the output node of second stage to be discharge before the completion of the evaluation phase of first stage.

The successive stage is evaluated concurrently, so the output node of the initial stage discharges[2] to VSS, but the output node of the second stage is incorrectly low at the end of the evaluation phase. As a result, this stage cannot be corrected. To overcome this problem, clocking schemes and modified circuit structure are required.

Domino CMOS logic

The charge redistribution and erroneous output of cascaded dynamic logic are avoided by inserting a static CMOS NOT logic gate between the cascadeddynamic logic structures, as illustrated in Figure 7. With the addition of a static inverter, the number ofdynamic CMOS logic stages that can be used in a cascade increases.

When the clock signal operates the circuit in the precharge stage, the output node of each stage is at a logic high level, while the output of the NOT gateis at a logic low level. This will disable the NMOS transistor of the next stage. Thus, the output node of the next stage is now evaluated conditionally

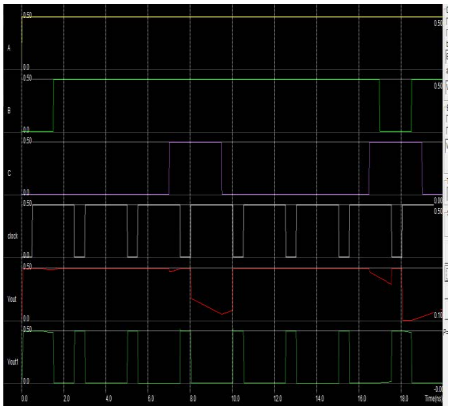

Figure 6: Timing simulation of Cascade Dynamic CMOS logic

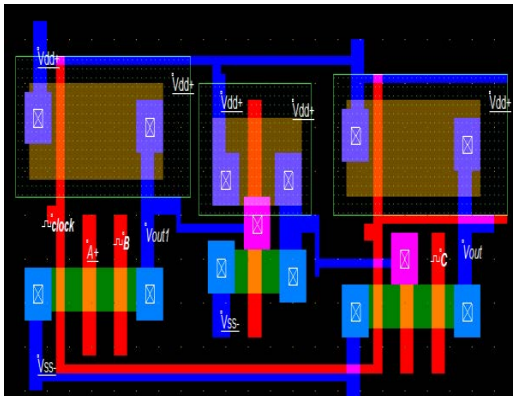

Figure 8: Layout Design of Domino CMOS logic

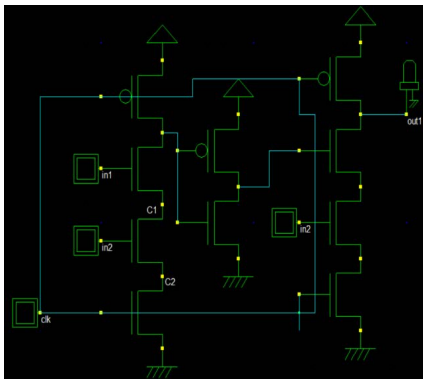

Figure 7: Schematic Design of Domino CMOS Logic

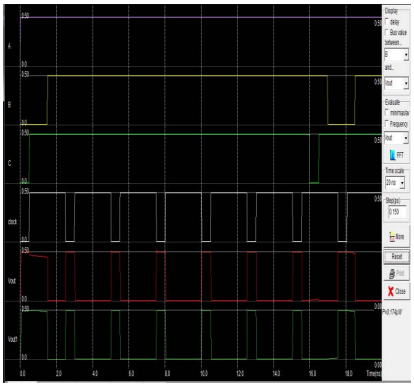

Figure 9: Timing simulation of Domino CMOS logic

based on the logic levels of the input node. In a multistage cascaded dynamic logic structure, theevaluated output node levels ripple the evaluation process of its successive stages, similar to a chain of dominoes falling one after the other. This is why the structure is known as domino CMOS logic.

Figure 8 depicts the layout design of domino CMOS logic via NOT logic gate. Because of the capacitance at each node, there may be problems with speed reduction and charge redistribution in cascaded dynamic logic, resulting in false output.

Consider the domino CMOS circuit depicted in Figure 7. The initial inputs are at zero, and theoutput nodes are in the discharge stage. The output capacitance C1 of the first stage was precharged to logic 1 during the clock signal at level 0, i.e. duringthe precharge[4] phase. When the time comes, signal at level 1 i.e. at the evaluation stage the both input in1, in 2 shown in Figure 7 is at logic 1 and in 3is at logic 0. The charge stored in the output capacitance of the starting stage is now shared by the second node capacitance C2, resulting in the charge-sharing phenomenon.[3]

After sharing between C1 and C2, the output node voltage becomes VDD/(1+C1/C2). In the evaluation phase, for example, if C1=C2, the outputvoltage becomes VDD/2. This level may be setincorrectly low depending on the capacitance ratio. Thus, the output voltage of the following inverter will switch high, indicating a logic error. Figure 9 depicts the timing simulation of domino logic circuit.

Again, the layout parameters for this logic are Channel Length (NMOS) is 0.075µm, PMOS 0.05 µm, Channel Width NMOS 0.125µm, PMOS 0.275, Rise Delay 0.003ns, Fall Delay 0.002ns and Power Dissipation is[5] 0.174µW.

This problem of charge redistribution can be minimized depending on the circumstances. By using a low gain weak p-transistor with a small channel width and length ratio, charge redistribution can be avoided. The internal pull down network is precharged by this weak p- transistor via the precharge node itself.

This may increase the design's overall size and complexity. Unless there is a strong pull down path between the output and ground, a weak PMOS allows the output node to drive at logic high. The weak PMOS with a low W/L ratio can be used to balance the leakage of the output node, turning on only when the precharge [6] node voltage is VDD and creating a feedback path. During the discharge phase, the output node will turn off this transistor.

NP Domino Logic

Improving domino CMOS logic structure by cascading the alternately composed structure of NMOS and PMOS transistors. Instead of an intermediate NOT gate, an

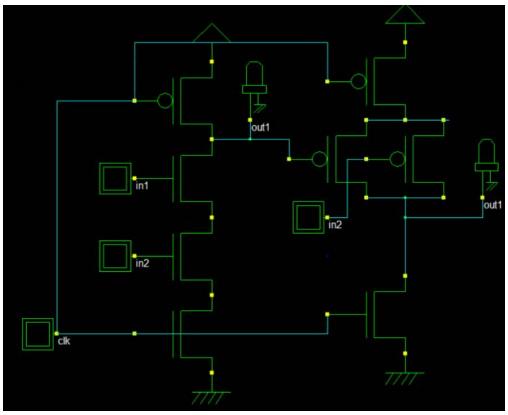

Figure 10: NPMOS Logic Schematic Design

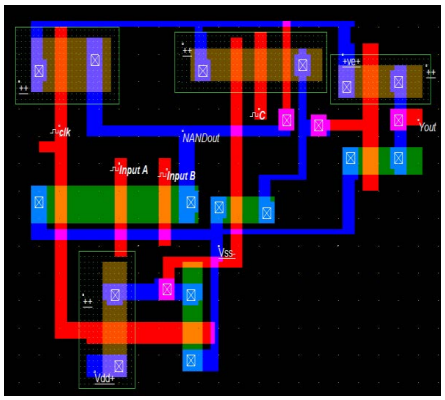

Figure 11: Layout Design of NP MOS Logic

alternate combination ofboth the transistors is used in this structure. Figure 10 depicts the NP MOS schematic structure, while Figure 11 depicts the layout design. The first stage of dynamic logic is designed with an NMOS pull down network, followed by a design with the PMOS pull-up network or vice versa. This structure will maximize the area of the circuit.

Because of the lower parasitic capacitances, thespeed will increase.

The following is how NORA CMOS logic works: The first stage (with NMOS logic) is prechargedhigh when clk = 0. The second stage (with PMOSlogic) has a low precharge. Similarly, the thirdstage (with NMOS logic) was precharged to a highlevel, and so on. When clk = 1, all cascaded NMOS and PMOS logic stages evaluate sequentially.

Design Layout for this logic is given as Channel Length for NMOS is 0.075 µm and PMOS is 0.05 µm), Channel Width for NMOS is 0.125 µm, PMOS is 0.275, Rise Delay is 0.007ns, Fall Delay is 0.002 ns and Power Dissipation[7] is 0.263µW

Zipper MOS Logic

Depending on the design constraints, an alternate structure of dynamic CMOS logic with NMOS pull down and PMOS pull up networks[8] is used to design the Zipper MOS logic shown in Figure 13.

The main concern of the NP Domino logic stage is that the requirement of an intermediate static inverter at each

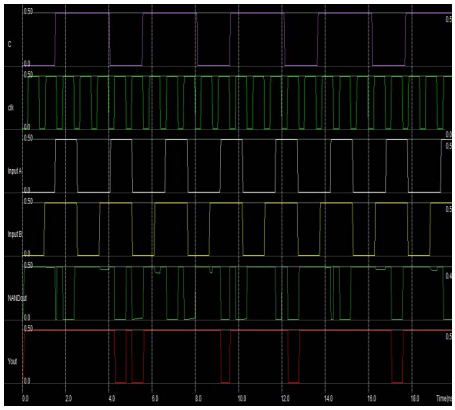

Figure 12: Timing Simulation of NPMOS logic

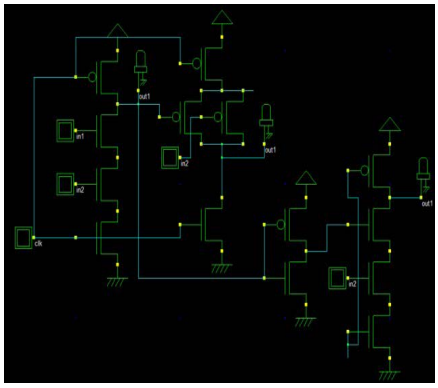

Figure 13: Schematic Diagram of Ziper Logic

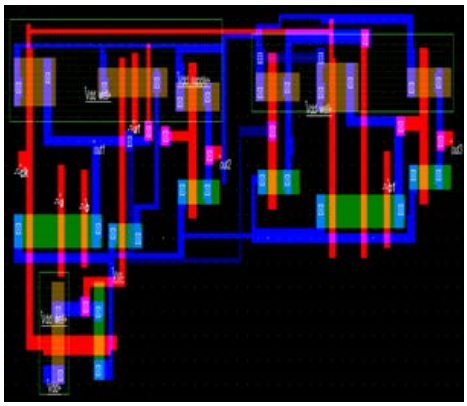

Figure 14: Layout Design of Zipper MOS Logic

stage output node of dynamic logic is avoided. Alternating both logic stages are designed instead of direct coupling of logic blocks. Zipper CMOS[9] logic is designed to optimize area, reduce parasitic capacitance, increase speed, and allow pipelined system architecture with glitch-free circuit.

Results and Discussions

After designing the circuits and analyzing it using the simulation tool graphical results are obtained which are shown below. The results obtained at the transistor nodes shows that power dissipation is very less in case of dynamic CMOS logics.

Various parameters are analyzed such as delay, area required, no. of transistors required for designing, power dissipation, etc.

As the structure becomes small power dissipation is of very prime concern in case of VLSI circuits as for high speed circuits the number of operations are large and for large time, it is critical that the power dissipation is to be kept to a minimum so that the overall circuit does not suffer damage.

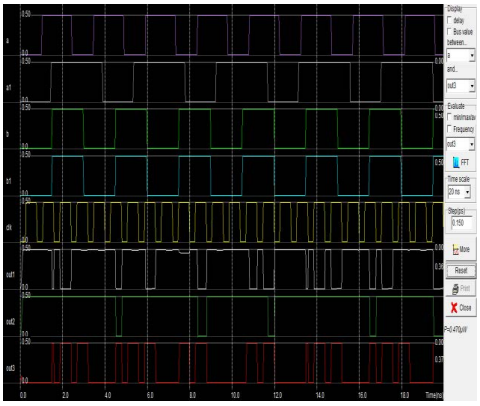

Figure 15: Timing Simulation of Zipper MOS logic.

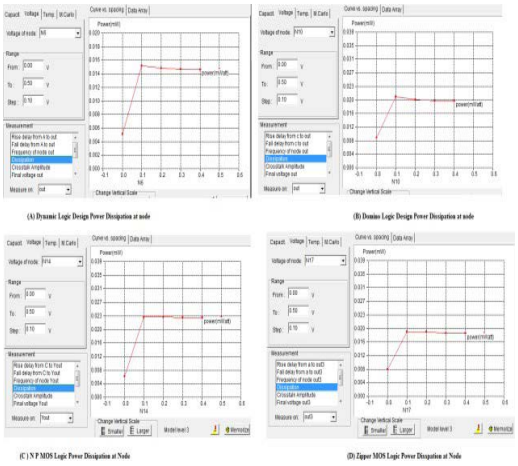

Figure 16: Graphical Analysis of Power Dissipation at Transistor nodes

Table 1: Performance Analysis of various parameters of different logics

S. No.	*Module design*	*Rise/Fall Delay*	*Power dissipation*	*Area overhead*
1.	Cascade dynamic cmos	0.003ns/0.002ns	0.174µw	8.5 Mm^2
2.	Domino Cmos logic	0.005ns/0.002ns	0.39µw	13.5 Mm^2
3.	Np domino logic	0.007ns/0.002ns	0.263µw	35 Mm^2
4.	Zipper Mos logic	0.007ns/0.002ns	0.466µw	76 Mm^2

Conclusion

Static CMOS logic designs with low voltage, low power circuits are often slow and are not useful in high-performance circuits. As a result, one of the better solutions for high-performance, low-area design circuits is to use dynamic CMOS logic. However, it has increased power dissipation. This paper describes methods for reducing dynamic power, leakage, and area while maintaining performance in application-specific integratedcircuits.

The mixed static and dynamic CMOS circuit overcome their own shortcomings by having a smaller area and a lower power dissipation thus making it a best choice for high-speed VLSI circuits.

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