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New Current-Mode Precision Full-Wave Rectifier Employing Single Inverted Z-Copy Current Differencing Buffered Amplifier

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Abstract

This paper aims to introduce a new current-mode precision full-wave rectifier configuration using a single inverted Z-copy current differencing buffered amplifier (IZC-CDBA) and two nMOSFETs. The unique feature of the proposed configuration is that it can simultaneously produce both the inverting and non-inverting rectified outputs without changing its architecture. Only active components make the configuration more suited for IC implementation. Moreover, it features low input impedance and high output impedance, making it fully cascadable. In addition, the new design enjoys extremely high-frequency operations. The effects of non-ideal transfer gain and parasitic impedances on the designed circuit are also explored. PSPICE simulations test the functionality of the proposed circuit for two distinct types of IZC-CDBA realization. The CMOS-based realization is checked through TSMC 0.18 µm level-7 technology parameters. The average DC current output, input dynamic range (± 450 µA), power consumption, temperature, total harmonic distortion, noise, and Monte-Carlo studies are performed to judge the efficiency level. The findings of the simulations match up nicely with the theoretical analysis. RMS and average value computation for a sinusoidal signal are also provided as an application of the suggested full-wave rectifier.

Keywords: Precision Full-Wave Rectifier, Current Differencing Buffered Amplifier (CDBA), Current-Mode and PSPICE.

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Introduction

A full-wave rectifier is an electrical device that transforms an alternating current into a pulsating direct current by using both halves of each cycle of the alternating current. They find wide applications in the field of analog signal processing, measurement, telecommunication, control engineering, and instrumentation, with applications in amplitude modulated (AM) signal detection, peak detection, signal polarity detection, ac to dc conversion, AC ammeters and voltmeters, linear function generators, watt meters, sample and hold circuits, clipper circuits, error measurements, function fitting, frequency doubling, and absolute value computation.[1-5] Classically, rectifiers were realized employing diodes and resistors. However, they can't rectify the signal below the diodes' threshold voltage. In order to overcome the threshold voltage issues for the rectification of low-level signals, which is critical for analog signal processing, a precision rectifier circuit based on an operational amplifier (op-amp) can also be implemented.[6,7] However, the output of an op-amp based rectifier is distorted due to the limited slew rate of the op-amp. Moreover, they are limited in the frequency range of operation because of the finite gain-bandwidth product. These flaws can be mitigated to some extent by using the current-mode approach as it provides a higher slew rate and larger gain-bandwidth product over their voltage-mode counterparts. Moreover, the current-mode brings advantages on performances like lower power consumption, greater linearity, higher dynamic range, temperature sensitivity and structural benefits such as circuit simplicity.[8,9]

Numerous precision full-wave rectifier designs employing different current-mode active building blocks namely, second generation current conveyor (CCII),[1-5] dual-X second generation current conveyor (DX-CCII),[5,10] dual-output second generation current conveyor (DO-CCII),[11] second-generation current controlled conveyor (CCCII),[12] multiple

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output current controlled current conveyor (MO-CCCII),[13] extra-X second generation current conveyor (EX-CCII),[14-16] current feedback operational amplifier (CFOA),[17] current differencing transconductance amplifier (CDTA),[18] modified Z-copy current difference transconductance amplifier (MZC-CDTA) [19], operational conveyor (OC),[20] operational transconductance amplifier (OTA),[21] differential voltage current conveyor (DVCC),[21,22] dual-output operational transconductance amplifier (DO-OTA),[23] operational transresistance amplifiers (OTRA),[24] floating current source (FCS),[25] operational floating current conveyor (OFCC) [26], differential difference current conveyors (DDCC),[27] differential voltage current conveyor transconductance amplifier (DVCCTA),[28] current differencing buffered amplifier (CDBA),[29] etc. have already been reported in literature. Unfortunately, these designs are not free from one or more of the following limitations:

- Uses multiple active devices.[1,4,13,17,20-22,24,28]
- Requirement of diodes.[1,3,5,21-23,25].
- Needed external resistor(s).[2,3,5,10,13,20-25,27]
- Operate in voltage-mode.[2,3,5,13,17,20,22,24,28]
- Uses three or more additional MOSFETs.[2,11,12,17,24,28]
- Cannot provide dual phase outputs from the same topology.[2-5,10,11,13,14,16-23,26-28]
- Requirement of comparatively large supply voltage.[1-5, 0-28]
- Operating frequency is comparatively low.[1-5,10-22,24, 26,28]
- Dissipate relatively large power.[2, 11-19, 22, 25-27]
- Employs mixed active devices.[1, 5, 13, 20]
- Unsuitable for fully cascadable operation.[1, 2, 10, 13, 17, 20-23, 25, 27, 28]
- Input dynamic range is comparatively low.[11, 14, 16, 19, 21, 25-27]
- Output is affected by temperature variation.[25]
- Output noise is comparatively large.[10, 12, 14, 15, 21]
- Offer high total harmonic distortion.[2, 10-16, 19]

The current differencing buffered amplifier (CDBA) has recently appeared as an alternative analog building block. There is a rising enthusiasm for CDBA and its derivatives. It offers all the profits of current-mode techniques and suitable for high-frequency operation. There are no internal parasitic capacitances at its input terminals as they are virtually grounded. Including a unity-gain current differencing amplifier and a unity-gain voltage amplifier allows it to be used in various current and voltage mode signal processing applications that demand higher speed, larger bandwidth and ease of implementation. Although analog signal processing circuits such as filters, oscillators, multipliers, inductor simulators, and others are voluminously available in literature employing CDBA or its derivatives as an active device, it is unfortunate that they have not yet been much explored as precision full-wave rectifiers. In,[29] a current-mode full-wave precision rectifier circuit has been reported using one CDBA and two diodes; however it requires a change in circuit topology to operate as a non-inverting and inverting rectifier. Furthermore, it can't operate at frequencies above 1 MHz and has a dynamic range of only ± 54 µA. Also, it requires a relatively large power supply. This has greatly influenced the authors to propose a new current-mode precision full-wave rectifier topology based on the new variant of CDBA called IZC-CDBA.

In this contribution, a new current-mode precision full-wave rectifier topology with low power supply and simple architecture is introduced, which is based on a single IZC-CDBA and two nMOSFETs. It can generate one inverting and one non-inverting rectified output from the same topology. In addition to this, the suggested rectifier possesses the following appealing features:

- Use of only one active device.
- No requirement of diodes.
- Resistorless realization.
- Fully cascadable.
- Eligible for low power system.
- Fit for IC implementation.
- Suitable for high-frequency operation.
- Offer low noise, low total harmonic distortion, and high dynamic range.
- Output is mostly temperature insensitive.

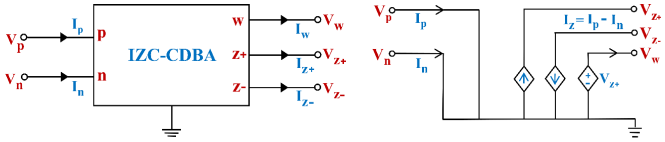
Description of Inverted Z-Copy Current Differencing Buffered Amplifier (Izc-Cdba)

Since the designed circuit is based on IZC-CDBA, a brief description of IZC-CDBA is given in this section. It resembles the CDBA in all perspectives with an additional *z* terminal, which is achieved by attaching an additional current inverter at the *z* terminal of the CDBA. The block diagram and the equivalent circuit of the IZC-CDBA are shown in Figure 1a and Figure 1b, respectively. The CMOS structure of IZC-CDBA is presented in Figure 2(a) which is a marginally modified version of the CDBA structure suggested in [30]. Figure 2(b) shows the IC AD844 based structure of the IZC-CDBA block.

The ideal terminal characteristics of the IZC-CDBA can be summarized as the following matrix equation:

$$\begin{bmatrix} V_p \\ V_n \\ V_w \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & -1 & 0 & 0 \\ -1 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_w \\ V_z \end{bmatrix} \quad (1)$$

The parameter g_m is the transconductance gain whose value depends on the bias current of MO-CCCCTA. The CMOS implementation of MO-CCCCTA is depicted in Figure 2.



(a) (b)

Figure 1: The IZC-CDBA building block (a) Block diagram (b) Equivalent circuit

Mathematical Model of the Proposed Precision Full-Wave Rectifier Circuit

Figure 3 illustrates the designed current-mode precision full-wave rectifier configuration. Two diode-connected-nMOSFETs and a single IZC-CDBA active device are used in this design. To comprehend how the suggested circuit works, one should first comprehend the OFF and ON states of the MOSFETs M_{D1} and M_{D2} in relation to the input signal. PSPICE simulation shows that when a 200 µA, 1 MHz sinusoidal signal is applied as input, the voltage at the x-node develops as depicted in Figure 4. Thus for each positive half-cycle of the input current, a negative voltage is developed at the x-node which turns the transistor M_{D1} ON while transistor M_{D2} remains OFF. The negative half-cycle of the input current makes the x-node voltage positive and turns the transistor M_{D2} ON & transistor M_{D1} OFF.

Hence, for $I_{in} \geq 0$; $I_p = +I_{in}$ and $I_n = 0$, thus using the port relationships of the IZC-CDBA active block it is found that:

$$I_{z+} = I_p = +I_{in} \text{ and } I_{z-} = -I_p = -I_{in} \quad (2)$$

Similarly, for $I_{in} \leq 0$; $I_p = 0$ and $I_n = -I_{in}$, thus from the port relationships of the IZC-CDBA device it is obtained that:

$$I_{z+} = -I_n = +I_{in} \text{ and } I_{z-} = I_n = -I_{in} \quad (3)$$

Therefore, form Equations (2) and (3), the outputs of the suggested precision full-wave rectifier circuitis obtained as follows:

$$I_{out+} = I_{z+} = +I_{in} \text{ and } I_{out-} = I_{z-} = -I_{in} \quad (4)$$

It is clear from Equation (4) that the proposed circuit acts as a current-mode precision full-wave rectifier. Equation (4) also reveals that the suggested circuit offers both the inverted and non-inverted rectified outputs simultaneously from the

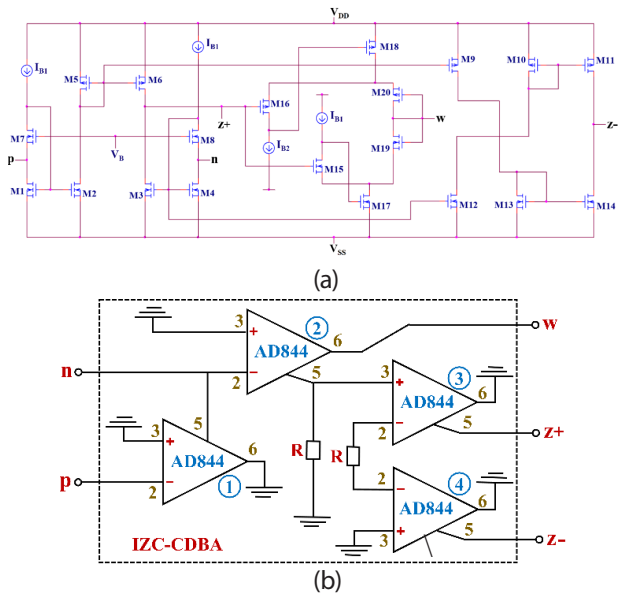


Figure 2: Internal structure of IZC-CDBA building block (a) CMOS based structure (b) IC AD844 based structure

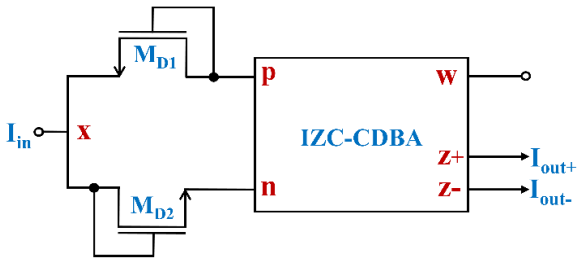


Figure 3: The proposed current-mode precision full-wave rectifier

terminals I_{out-} and I_{out+} respectively without any alternation of circuit topology.

Effect of Tracking Errors and Parasitic Impedances on the Proposed Rectifier Circuit

The analysis in the preceding section is built on the ideal behavior of the IZC-CDBA. Practically, the presented circuit departs from its optimal performance because of the current/voltage tracking errors and parasitic impedances in IZC-CDBA. Considering the current/voltage tracking errors, the terminal relationships of IZC-CDBA can be characterized as follows:

$$\begin{bmatrix} V_p \\ V_n \\ V_w \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \hat{a} \\ \acute{a}_{p+} & -\acute{a}_{n+} & 0 & 0 \\ -\acute{a}_{p-} & \acute{a}_{n-} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_w \\ V_z \end{bmatrix} \quad (5)$$

where $\acute{a}_{p+} = 1 - \mathring{a}_{p+}$ and $\mathring{a}_{p+}(|\mathring{a}_{p+}| \ll 1)$ is the current tracking error from *p* terminal to *z* terminal, $\acute{a}_{n+} = 1 - \mathring{a}_{n+}$ and $\mathring{a}_{n+}(|\mathring{a}_{n+}| \ll 1)$ is the current tracking error from *n* terminal to *z* terminal, $\acute{a}_{p-} = 1 - \mathring{a}_{p-}$ and $\mathring{a}_{p-}(|\mathring{a}_{p-}| \ll 1)$ is the current tracking error from *p* terminal to *z* terminal, $\alpha_{n-} = 1 - \varepsilon_{n-}$ and $\varepsilon_{n-}(|\varepsilon_{n-}| \ll 1)$ is the current tracking error from *n* terminal to *z* terminal, and $\hat{a} = 1 - \mathring{a}_v$ and $\mathring{a}_v(|\mathring{a}_v| \ll 1)$ is the voltage tracking error from *z* terminal to *w* terminal of the IZC-CDBA block.

Taking into account the above non-ideal gain values, a reanalysis of the designed rectifier gives:

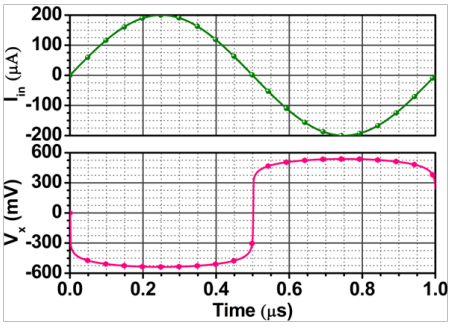


Figure 4: Time domain response of input current (I_{in}) and x-node voltage (V_x)

$$I_{out+} = \alpha_{p+} I_p - \alpha_{n+} I_n \text{ and } I_{out-} = -\alpha_{p-} I_p + \alpha_{n-} I_n \quad (6)$$

During the positive cycle:

$$I_{in} \geq 0 : I_p = +I_{in} \text{ and } I_n = 0$$
$$I_{out+} = \alpha_{p+} I_{in} \text{ and } I_{out-} = -\alpha_{p-} I_{in} \quad (7)$$

During the negative cycle:

$$I_{in} \leq 0 : I_p = 0 \text{ and } I_n = -I_{in}$$
$$I_{out+} = \alpha_{n+} I_{in} \text{ and } I_{out-} = -\alpha_{n-} I_{in} \quad (8)$$

In the ideal circumstances, these gains are unity and Equations (7) & (8) reduced to Equations (2) & (3), respectively. However, it is noted from Equations (7) and (8) that the peak amplitude of the rectified output signals during the positive and negative input signals is affected by the non-idealities, as they now depend on current transfer gains α_{p+}, α_{p-}, α_{n+}, and α_{n-}.

Furthermore, a practical IZC-CDBA exhibits various terminal parasitics like any other active device. Figure 5 depicts the parasitic model of the IZC-CDBA. A parasitic resistor R_p appears in series at *p* terminal, series parasitic resistance R_n appears at *n* terminal, parasitic resistance R_o appears in series at *w* terminal, parasitic impedances in the form of $R_{z+}||C_{z+}$ appears at *z* terminaland $R_{z-}||C_{z-}$ appears at *z* terminal. All the parasitic capacitors are of very small values while resistor R_p, R_n, and R_o are of very small values and resistor R_{z+} and R_{z-} are of high values. Considering the parasitics, the voltage developed at the p and n nodes of the proposed circuit are $I_p{*}R_p$ and $I_n{*}R_n$, respectively.

During the positive cycle, M_{D1} transistor is ON while M_{D2} transistor is OFF. As a result, the resistance at the *p* and *n* terminals is the series combination of resistance R_p and the resistance associated with the M_{D1} (ON) transistor and the series combination of resistance R_n and the resistance associated with the M_{D2} (OFF) transistor, respectively,. In light of the preceding premise, Figure 6 depicts the equivalent circuit obtained from Figure 3.

Hence, the total input resistance is the parallel combination of R_p in series with R_{ON} (resistance associated with M_{D1} when it

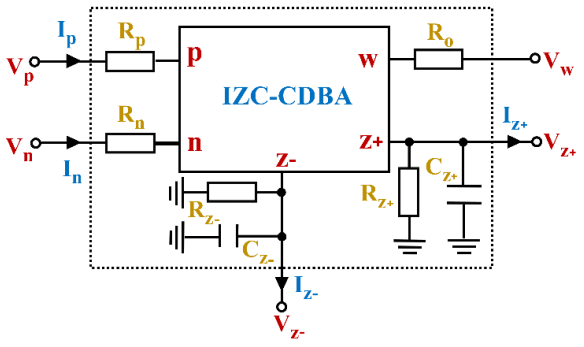


Figure 5: Parasitic model of IZC-CDBA

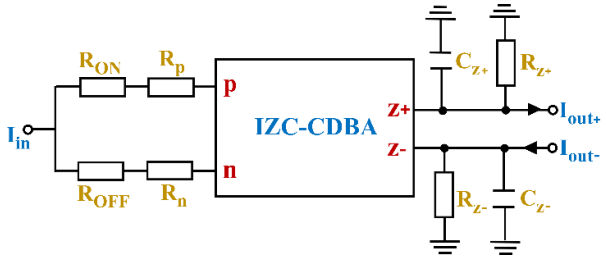


Figure 6: Equivalent circuit reveals parasitics during positive cycle

is in ON state) and R_n in series with R_{OFF} (resistance associated with M_{D2} when it is in OFF state). Thus, no additional buffer is required for the current input signal circuit. Similar result is obtained during the negative cycle, but the resistances MD1 and MD2 are swapped in this case.

Pspice Simulation Results

To justify the theoretical anticipations, the designed current-mode full-wave precision rectifier circuit in Figure 3 has been simulated with the SPICE program. Initially, the suggested circuit's effectiveness has been investigated using the CMOS structure of IZC-CDBA. To assist in the hardware implementation of the reported full-wave rectifier, the IZC-CDBA block has also been built using market available ICs AD844 and the PSPICE simulation results for this have been reported subsequently. The simulations are accomplished by using TSMC 0.18 µm CMOS (level-7) technology parameters. The external NMOS transistors M_{D1} and M_{D2} are selected with dimensions having aspect ratios 0.8 µm/0.18µm.

Simulation Results Using CMOS Structure of IZC-CDBA

The CMOS based IZC-CDBA structure used in the simulation process is depicted in Figure 2(a), with DC power supply voltages $V_{DD} = -V_{SS} = 0.6$ V and bias voltage $V_B = 0.45$ V. The biasing currents I_{B1} and I_{B2} are chosen as 50 µA and 80 µA, respectively. Table 1 presents the dimensions of various transistors used in the CMOS based IZC-CDBA structure. The performance parameters of the CMOS based IZC-CDBA are measured and listed in Table 2.

The DC transfer characteristics for the non-inverting and inverting output of the suggested full-wave rectifier are shown in Figures 7(a) and (b), respectively. Its input dynamic range is estimated to be ± 450 µA. The magnified zero crossing region of the DC transfer characteristics is demonstrated in Figure 8. The offset value for the non-inverting output is 165 nA, whereas for the inverting output it is 157 nA. Figure 9 depicts the current outputs of the proposed full-wave rectifier at different frequencies. These simulations use sinusoidal current signals of 150 µA peak value and different frequencies of 100 kHz, 1 MHz, 50, 100, 150, and 200 MHz are he The plot shows that the suggested full-wave rectifier operates well above 100 MHz, although the zero crossing distortion worsens as the frequency approaches

Table 1: The dimensions of the MOS transistors used in the IZC-CDBA structure

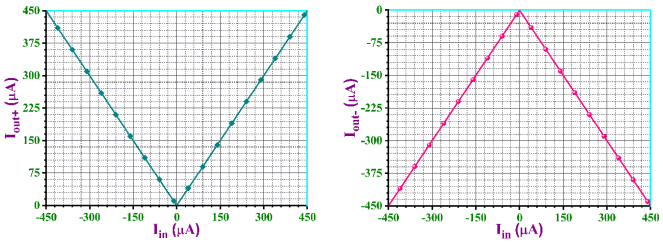
Transistors	*W/L (μm/μm)*
M_1, M_2, M_3, M_4	3.6/1.80
M_5, M_6, M_7, M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}	90/1.80
M_{15}	45/0.36
M_{16}, M_{18}, M_{20}	126/0.36
M_{17}, M_{19}	72/0.36

Table 2: Simulated performance parameters of the CMOS based IZC-CDBA structure

Performance parameters	*Values*
Terminal-p resistance	56 Ω
Terminal-n resistance	56 Ω
Terminal-w resistance	270 Ω
Terminal-z+ resistance	157 kΩ
Terminal-z– resistance	157 kΩ
Current transfer ratio, $\alpha_+ = I_{z+}/(I_p - I_n)$	0.985
Current transfer ratio, $\alpha_- = I_{z-}/(I_p - I_n)$	0.987
Current transfer bandwidth	459 MHz
Voltage transfer ratio, $\beta = V_w/V_z$	0.978
Voltage transfer bandwidth	974 MHz

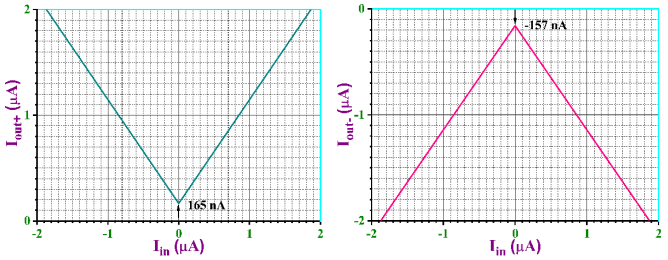
200 MHz, yet it remains within acceptable limits. Hence, it can be concluded that the reported full-wave rectifier can operate up to a very high frequency of 200 MHz. The time-domain performance of the proposed full-wave rectifier for sinusoidal input currents having amplitudes of 50 μA, 100 μA, 200 μA, and 300 μA at 1 MHz frequency is also tested. The corresponding results are presented in Figure 10. The designed circuit dissipates only 0.318 mW power.

The proposed rectifier circuit is simulated for three different temperatures of 25, 50, and 100°C using a 200 μA, 1 MHz sinusoidal input signa to study temperature effectl. Figure 11 illustrates the comparable outcomes. Clearly, the



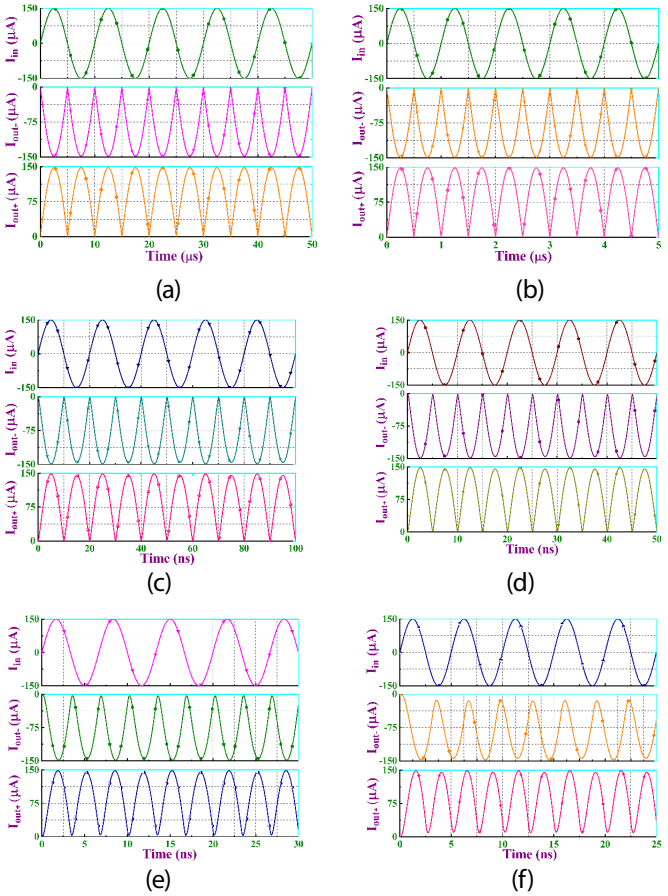
(a) (b)

Figure 7: DC transfer characteristics of the suggested full-wave rectifier circuit with CMOS based IZC-CDBA (a) Non-inverting output (b) Inverting output



(a) (b)

Figure 8: DC transfer characteristics near zero crossing region of the suggested rectifier circuit with CMOS based IZC-CDBA (a) Non-inverting output (b) Inverting output



(a) (b) (c) (d) (e) (f)

Figure 9: Simulated rectified outputs of the suggested rectifier with CMOS based IZC-CDBA at different frequencies in dual phase for input current of 150 μA peak value (a) 100 kHz (b) 1 MHz (c) 50 MHz (d) 100 MHz (e) 150 MHz (f) 200 MHz

responses are largely unaffected by temperature changes. So, there is no requirement of any temperature compensatory circuit. RMS error () and DC value transfer () are calculated to assess the accuracy of the derived rectifier. Mathematically, they are formulated as follows:

$$\tilde{n}_{RMS} = \sqrt{\frac{\int_T \left[I_{oa}(t) - I_{oi}(t)\right]^2 dt}{\int_T I_{oi}^2(t)\,dt}} \text{ and } \tilde{n}_{DC} = \frac{\int_T I_{oa}(t)\,dt}{\int_T I_{oi}(t)\,dt} \quad (9)$$

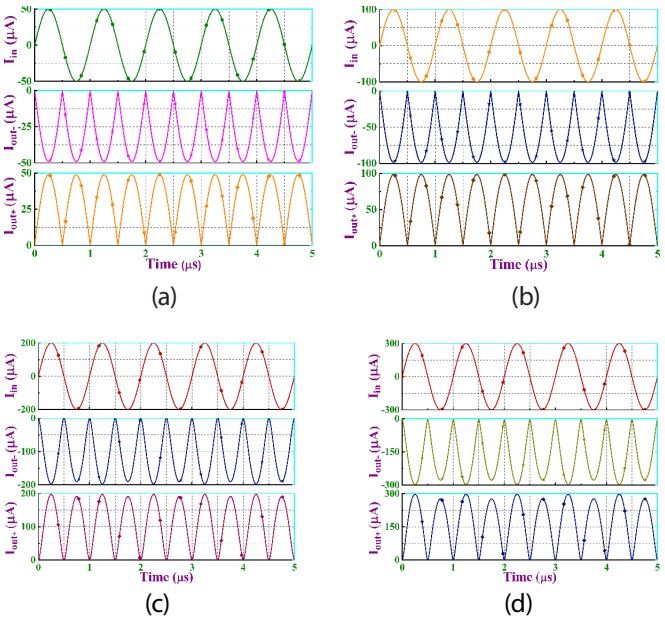


Figure 10: Simulated rectified outputs of the suggested full-wave rectifier circuit with CMOS based IZC-CDBA for different input current amplitudes in dual phase at 1 MHz frequency (a) 50 μA (b) 100 μA (c) 200 μA (d) 300 μA

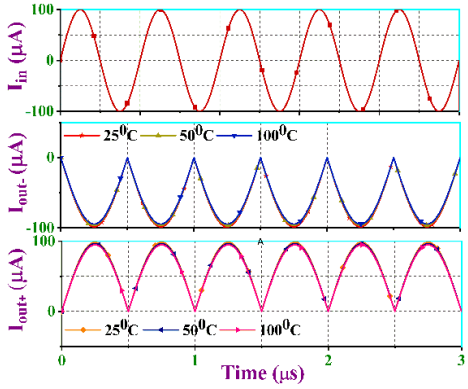


Figure 11: Simulated responses at different temperatures for the designed full-wave rectifier with CMOS based IZC-CDBA

where denotes the ideal output value and denotes the actual output value. The ideal values for and are 1 and 0, respectively. The variation in simulated against the frequency variation is presented in Figure 12 whereas Figure 13 plots the variation in simulated against the frequency variation. The designed rectifier can clearly be utilized for extremely high-frequency, as indicated in Figures 12 and 13 are consistent with the findings achieved in Figure 9.

Figure 14 depicts the average output current for the designed full-wave rectifier, which is found to be ± 95.32 μA, close to the expected value of $2(I_p/\pi) = \pm 95.45$ μA, where I_p = 150 μA. The reported rectifier circuit is also sorely tested to detect the level of harmonic distortion at the signal's output. Figure 15 displays the variation of total harmonic distortion

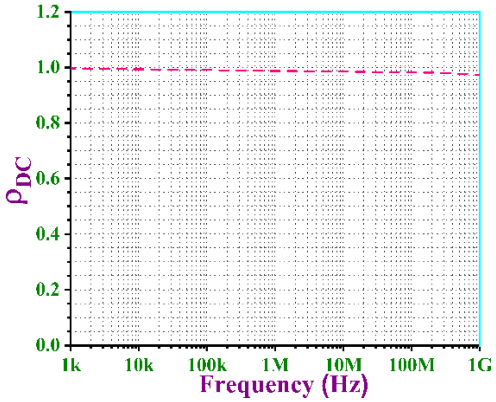


Figure 12: Simulated vs frequency curve for the designed full-wave rectifier with CMOS based IZC-CDBA

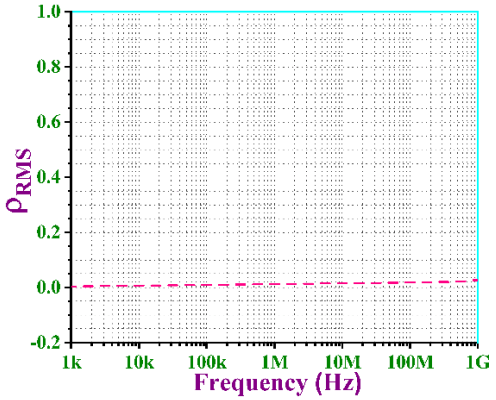
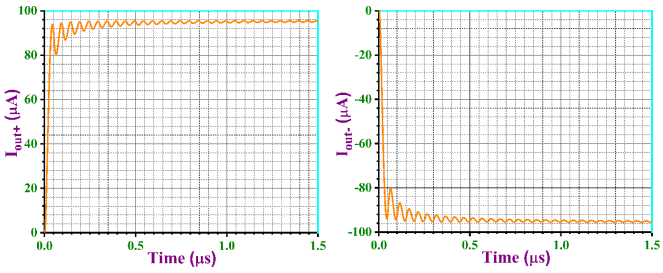


Figure 13: Variation of simulated with frequency for the designed full-wave rectifier with CMOS based IZC-CDBA

(THD) as a function of frequency. It is to be seen that THD is below – 30.2 dB over the entire frequency range for a 200 μA input signal. Output noise behavior of the recommended rectifier is also judged in terms of frequency variation. The corresponding result is plotted in Figure 16 when a 1 kΩ resistor is connected to the circuit's output. It is to be seen that output noise is constant and as low as 4.89 nV/√Hz upto 100 MHz frequency and decreases more for higher frequencies.

The effect of threshold voltage on the rectifier output is also investigated by using the well-known Monte-Carlo analysis. The histograms of the peak amplitude of output currents, for a 200 μA, 1 MHz sinusoidal input, for 100 runs with a 1% variance in the threshold voltage and transconductance of all MOSFETs are depicted in Figure 17. The results show that the mean value of the distribution of peak amplitude for non-inverting output is 199.948 μA with a standard deviation 83.95 nA and –199.903 μA with standard deviation 225.43 nA for inverting output. Hence, it can be inferred that the effect of threshold voltage on the proposed structure is not significant.



(a) (b)

Figure 14: Average DC current output of the proposed full-wave rectifier with CMOS based IZC-CDBA for dual phase (a) Non-inverting output (b) Inverting output

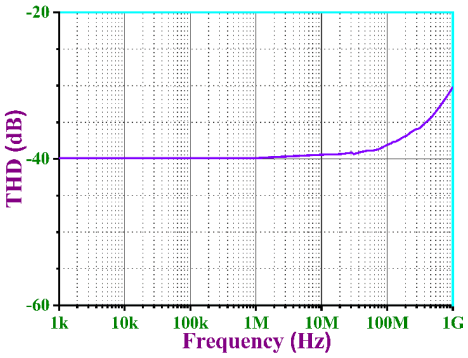


Figure 15: Variation of THD of the proposed full-wave rectifier as a function of frequency with CMOS based IZC-CDBA

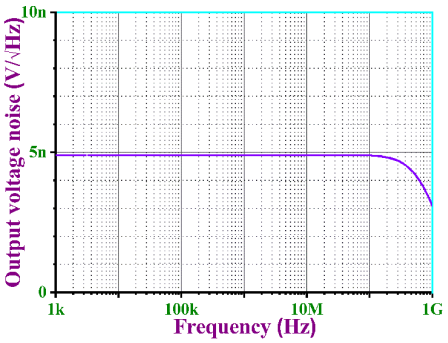


Figure 16: Variation of output noise of the proposed full-wave rectifier against frequency with CMOS based IZC-CDBA

Simulation Results Using IC AD844 Based Structure of IZC-CDBA

The effectiveness of the devised full-wave rectifier is also judged by employing the commercially available ICs AD844 based structure of IZC-CDBA block. The realization of IZC-CDBA block using four AD844 ICs is demonstrated in Figure 2(b). Supply voltages are taken as ± 5 V. As per the recommendation in the datasheet, a small series resistance of 4.7 Ω is included in each supply line. The DC transfer characteristics for the suggested full-wave rectifier's non-inverting and inverting output are shown in Figures 18(a) and (b), respectively. Its input dynamic range is estimated to be ± 15mA. The magnified zero-crossing region of the

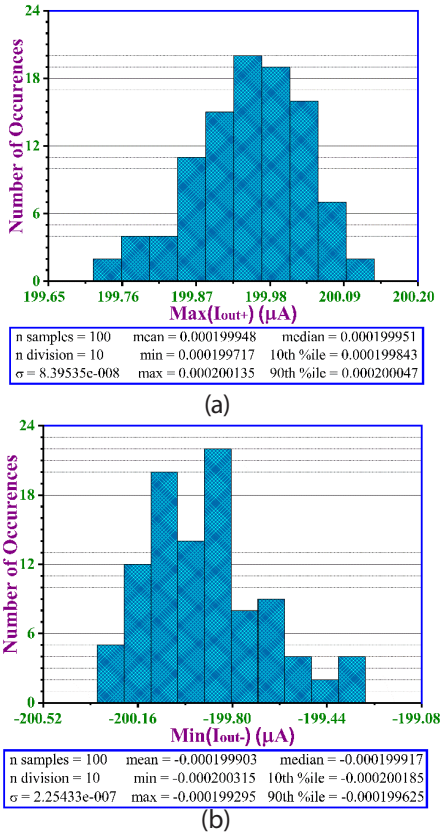


Figure 17: Monte-Carlo simulation results of the proposed rectifier employing CMOS based IZC-CDBA for 100 samples with (a) 1% variance in threshold voltage and transconductance of all MOSFETs (a) Non-inverting output (b) Inverting output

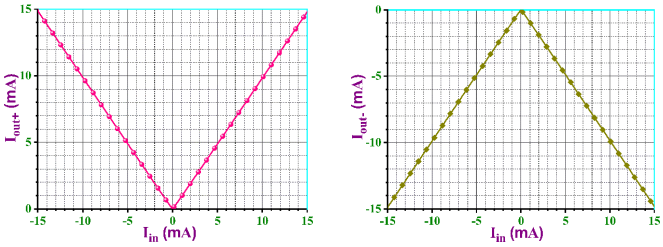
DC transfer characteristics is demonstrated in Figure 19. The offset value for the non-inverting output is 16.28 pA, whereas it is – 21.65 pA for the inverting output. Figure 20 depicts the current outputs of the proposed full-wave rectifier at different frequencies. These simulations use sinusoidal current signals of 1 mA peak value and different frequencies of 100 kHz, 1 MHz, 5, and 10 MHz as input signals. The time-domain performance of the proposed full-wave rectifier for sinusoidal input currents with amplitudes of 0.1, 0.5, 5, and 10 mA at 1MHz frequency is also tested an.

Application of the Proposed Rectifier as an Average and RMS value computator

There are various uses for the rectifier. Obtaining root-mean-square (RMS) and average values for a sinusoid electrical signal is one of the applications of the suggested rectifier (Figure 21). The average and RMS value of a signal is defined as follows:

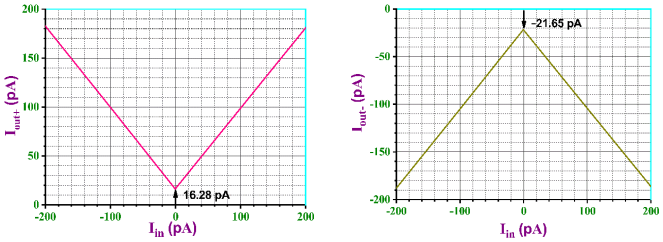
$$I_{avg} = \frac{1}{T}\int_0^T |I(t)|dt \text{ and } I_{RMS} = \sqrt{\frac{1}{T}\int_0^T I^2(t)dt} \quad (10)$$

where I(t) is the AC current signal, T is its time period, and I_{avg} & I_{RMS} is the average & RMS value of the rectified I(t) signal,



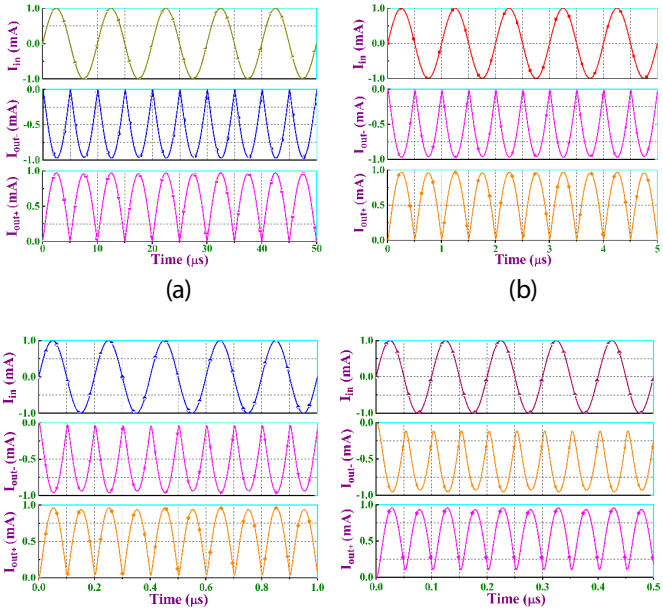
(a) (b)

Figure 18: DC transfer characteristics of the suggested full-wave rectifier circuit with AD844 based IZC-CDBA (a) Non-inverting output (b) Inverting output



(a) (b)

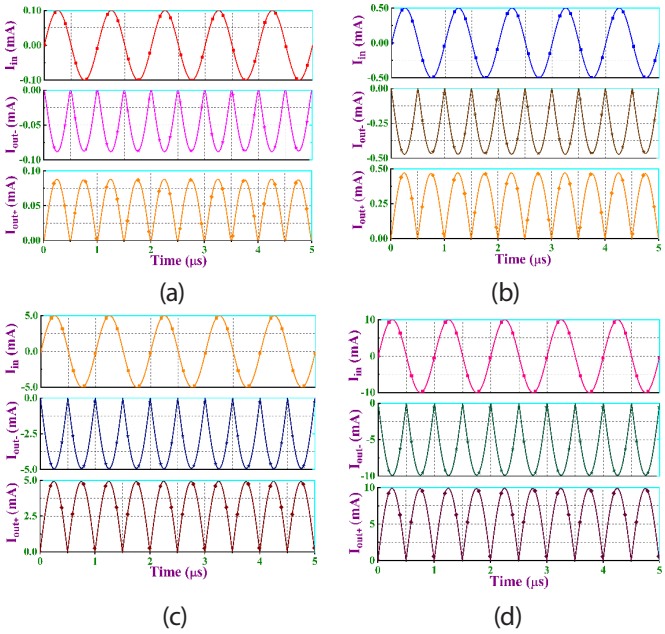
Figure 19: DC transfer characteristics near zero crossing region of the suggested rectifier with AD844 based IZC-CDBA (a) Non-inverting output (b) Inverting output



(a) (b) (c) (d)

Figure 20: Simulated rectified outputs of the suggested full-wave rectifier circuit with CMOS based IZC-CDBA at different frequencies in dual phase for input current of 1 mA peak value (a) 100 kHz (b) 1 MHz (c) 5 MHz (d) 10 MHz

respectively. In order to execute this operation, the AC signal is rectified first and then passes through a low-pass filter. In the case of a sinusoidal signal I(t) = I_p sin(2πft), where I_p denotes maximum amplitude and f denotes frequency, the average and RMS values of I(t) is measured as follows:



(a) (b) (c) (d)

Figure 21: Simulated rectified outputs of the suggested full-wave rectifier circuit with AD844 based IZC-CDBA for different input current amplitudes in dual phase at 1MHz frequency (a) 0.1 mA (b) 0.5 mA (c) 5 mA (d) 10 mA

$$I_{avg} = \frac{2}{\delta} I_p = 0.637 I_p \text{ and } I_{RMS} = \frac{1}{\sqrt{2}} I_p = 0.707 I_p \quad (11)$$

From Equation (11) it is clear that the ratio of RMS and average value of I(t) is calculated to be:

$$\frac{I_{RMS}}{I_{avg}} = \frac{0.707 I_p}{0.637 I_p} = 1.11 \quad (12)$$

This is the amount of amplification needed to obtain I_{RMS} from I_{avg}. In line with,[15] the designed rectifier can be used to determine the average and RMS values for sinusoid electric signal, as illustrated in Figure 22. A first-order low pass filter is achieved by proper selection of the parameters of NMOS transistor M_{E1} and the value of capacitor C. The rectifier's output current (I_{out}) is supplied to the filter's input, where the signal's ac components are filtered through capacitor C and the DC component enters the transistor M_{E1}, which is subsequently replicated by the M_{E2} and M_{E3} current mirror MOS transistors. The average current I_{avg} can be obtained at the drain of M_{E2} by selecting the transistor M_{E1} and M_{E2} identical. As Equation (12) indicates, I_{RMS} is obtained at the drain of M_{E3} by adopting $g_{mE3}/g_{mE1} = 1.11$, where g_m denotes the relevant transistor's transconductance. The value of the capacitor must be high enough to keep the ripple under control. To put it another way,

$$C >> \frac{g_{max}}{4\delta f_{min}} \quad (13)$$

Table 3: Comparison between the suggested and previously reported full-wave rectifier circuits [1-5, 10-29]

Ref./ Year	*Active device*	*Transistor count*	*Number of additional MOS/diode*	*Number of resistor*	*Cascadability*	*Supply voltage (Volt)*	*o/p type*	*Operating frequency (MHz)*	*Power consume (mW)*	*Noise (nV/ √Hz)*	*Technology (µm)*	*I/p dynamic range*	*Temperature stability*	*THD (dB)*
[1]/2011	1 CCII+ 1 UVC	NR	0/2	0	No	NR	S	1	NR	NR	NR	NR	NR	NR
	2 CCII	NR	0/2	0	No	NR	D	1	NR	NR	NR	NR	NR	NR
[2]/2014	1 CCII	10	28/0	2	No	± 1.2	D	100	5.2	NR	0.18	±250 mV	Yes	–13
[3]/2017	1 CCII-	NR	0/2	2	Yes	± 1.65	S	0.01	NR	NR	0.35	±400 mV	NR	NR
[4]/2019	2 CCII	30	0/0	0	Yes	± 0.9	S	0.2	NR	NR	0.18	NR	Yes	NR
[5]/2013	1 CCII+1 DX-CCII	29	0/2	2	Yes	± 2.5	S	83	NR	NR	0.35	±400 mV	NR	NR
[10]/2019	1 DX-CCII	22	2/0	2	No	± 1.25	S	50	NR	36.94	0.13	NR	NR	–11.6
[11]/2018	1 DO-CCII	22	12/0	0	Yes	± 0.9	S	1	0.188	NR	0.18	±0.1 mA	Yes	–15.7
[12]/2020	1 CCCII	19	4/0	0	Yes	± 1.5	D	30	1.07	5.4	0.35	±1 mA	Yes	–16.3
[13]/2017	1 MO-CCCII +1 ZCD +1 SW	27	0/0	2	No	± 1.2	S	10	2.83	NR	BJT	±80 mV	NR	–20.8
[14]/2017	1 EX-CCII	27	2/0	0	Yes	±1.25	S	10	0.3	6.4	0.25	±0.2 mA	Yes	–10
[15]/2020	1 EX-CCII	36	2/0	0	Yes	± 1.25	D	125	0.62	6.5	0.18	±0.5 mA	Yes	–7.52
[16]/2020	1 EX-CCII	21	2/0	0	Yes	± 0.9	S	30	0.2	6.7	0.13	±0.3 mA	Yes	–12.3
[17]/2017	2 CFOA	36	3/0	0	No	± 1.25	S	1	1.33	NR	0.25	±350 mV	Yes	NR
[18]/2014	1 CDTA	21	2/0	0	Yes	± 1.5	S	100	1.12	3.52	0.18	±2 mA	NR	NR
[19]/2013	1 MZC-CDTA	28	2/0	0	Yes	± 1.8	S	0.01	14	NR	0.35	± 0.3 mA	NR	–13.15
[20]/2020	1 OC + 4 CM	33	0/0	7	No	± 10	S	0.1	NR	NR	BJT	± 10 mV	NR	NR
[21]/2016	1 OTA	8	0/2	2	No	± 1.5	S	1	NR	12	0.25	± 0.2 mA	Yes	NR
	1 DVCC	12	0/2	3	No	± 1.5	S	1	NR	20	0.25	± 0.2 mA	Yes	NR
[22]/2016	2 DVCC	24	0/2	2	No	± 1.25	S	1	0.93	NR	0.25	±170 mV	Yes	NR
[23]/2010	1 DO-OTA	20	0/4	1	No	± 5	S	300	NR	NR	0.25	± 0.5 mA	Yes	NR
[24]/2017	3 OTRA	42	6/0	8	Yes	± 2.5	D	0.001	NR	NR	0.18	NR	Yes	NR
[25]/2017	1 FCS	4	0/2	2	No	± 0.75	D	500	0.8	NR	0.18	± 0.1 mA	No	NR
[26]/2014	1 OFCC	36	2/0	0	Yes	± 1.8	S	0.3	0.432	NR	0.18	± 0.04 mA	NR	NR
[27]/2021	1 DDCC	14	2/0	3	No	± 0.9	S	200	2.94	NR	0.18	± 0.3 mA	NR	NR
[28]/2021	2 DVCCTA	46	5/0	0	No	± 1.5	S	1	NR	NR	0.18	±200 mV	NR	NR
[29]/2015	1 CDBA	20	0/2	0	Yes	± 1.5	S	1	NR	NR	0.25	± 0.054 mA	NR	NR
This work	1 IZC-CDBA	20	2/0	0	Yes	± 0.6	D	200	0.318	4.89	0.18	± 0.45 mA	Yes	–30.2

UVC = Universal voltage conveyor; ZCD = Zero-crossing detector; SW = Switch; CM = Current mirror; NR = Not reported; S = Single phase; D = Dual phase

where f_{min} is the lowest frequency of interest and g_{max} is the maximum transconductance value.

To simulate the circuit shown in Figure 22, the power supply, biasing voltage and biasing currents of the CMOS based IZC-CDBA are chosen the same as in Section 5.1. The dimensions of different MOSFETs in the CMOS based IZC-CDBA and diode-connected MOS transistors (M_{D1} and M_{D2}) are used as before. The aspect ratios of external MOSFETs M_{E1}, M_{E2} and M_{E3} are chosen as $(W/L)_{ME1} = (W/L)_{ME2} = (23\ \mu m/1.8\ \mu m)$ and $(W/L)_{ME3} = (25.53\ \mu m/1.8\ \mu m)$. The value of capacitor C is chosen as 1.8nF and a 100µA, 1MHz sinusoidal current signal is fed to the input of the circuit. The corresponding simulation results are shown in Figure 23. As expected, the I_{avg} and I_{RMS} are found as 63.64 µA and 70.64 µA, respectively, with a ripple of around 0.85 percent.

Comparison with Recently Reported Full-Wave Rectifiers

The performance parameters of the designed rectifier are summarized and compared with other previously published related works[1-5,10-29] in Table 3. It depicts that of all the circuits given in Table 3 the designed rectifier needed least power supply and offer lowest noise and better total harmonic distortion. Although references[12,15,18,23] provide a comparatively higher input dynamic range than the proposed structure, the maximum operating frequency for the circuits of references[12,15,18] are relatively low. Moreover, they dissipate relatively large power. Again, the circuit of Ref.[27] is not fully cascadable. Furthermore, it employs four diodes and one external resistor. Though references[11,14,16] consume relatively lower power than the reported circuit, their maximum operating frequency is also comparatively low. The circuit of Ref.[25] offers higher operating frequency, but to achieve this, one must pay for power consumption and input dynamic range. In spite of that it is not fully cascadable and employs external resistors. Evidently, none of the references mentioned in Table 3 can simultaneously achieve the advantageous features of the proposed rectifier, i.e., simple architecture, low component count, capability of delivering dual phase outputs without any change in circuit topology, low power dissipation, higher input dynamic range, low supply voltage, suitable for fully cascadation, low noise, fit for IC implementation, and low THD, thus justifying the design proposal.

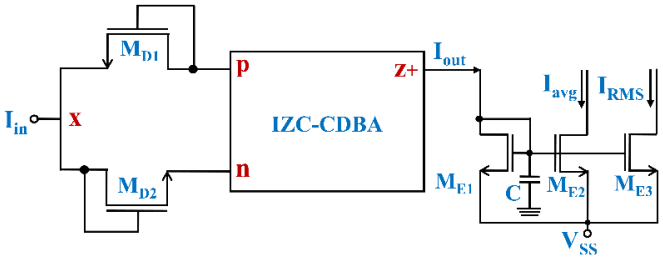


Figure 22: The proposed full-wave rectifier based average and RMS value computation circuit for sinusoidal wave

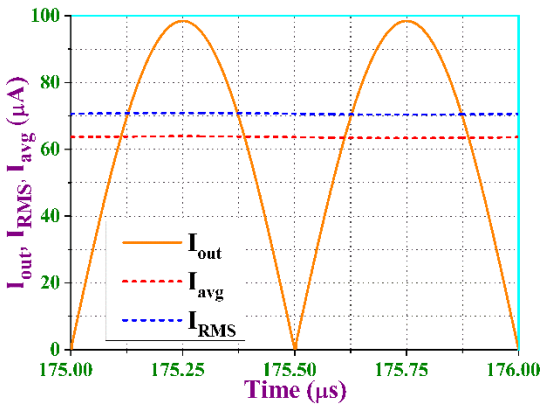


Figure 23: Simulated I_{out} (rectified), I_{RMS} and I_{avg} for a 100 µA, 1 MHz sinusoidal input with CMOS based IZC-CDBA

Conclusion

The prime focus of this research study was to design a new current-mode precision full-wave rectifier configuration utilizing a single IZC-CDBA and two nMOSFETs. The derived circuit offers dual phase rectified outputs from the same topology at the same time. The configuration is better suitable for IC implementation as only active components are used. It also has low input impedance and high output impedance, allowing it to be fully cascaded. Furthermore, the new architecture is appropriate for extremely high-frequency operations. Other significant metrics such as power consumption, input dynamic range, THD, output noise, temperature stability, and Monte Carlo analysis also show good results. PSPICE simulation results obtained by employing CMOS as well as AD844 based structure of IZC-CDBA and the TSMC 0.18 µm technology parameters agree well with the theoretical proposition. The sinusoidal to RMS and average conversation is also demonstrated as an application of the devised precision full-wave rectifier.

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