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Optimizing and Recuperating the Leakages in Low Voltage CMOS Circuits

Ambresh Patel, Ritesh Sadiwala*

Department of Electronics and Communication Engineering, RKDF University, Gandhinagar, Bhopal-462003, Madhya Pradesh, INDIA

Abstract

With the advancement of technology, small and handy electronic devices are built with low supply voltage and lower power dissipation in designing deep submicron static CMOS circuits. Small devices scaling down with burst-mode type integrated circuits have two major challenges: area and power dissipation. This paper presents a method for decreasing dynamic power, area, and leakage of application-specific integrated circuits without sacrificing performance. The High Threshold Leakage Control Transistor, TG-Based Technique, Supply Voltage Scaling, Sleep Transistor approaches are covered, and a dynamic CMOS architecture with stack transistor. With certain area and delay considerations, these strategies are utilized to diminish both types of power dissipation in the CMOS logic designs.

Keywords: CMOS, High threshold, Leakage, TG-based technique.

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Introduction

An electronic appliance that has triggered some Low power VLSI circuit design is the focus of the study. The operational time of a battery-powered electronic system is severely constrained by the battery backup time. In electronic systems, the requirement for power dissipation reduction varies based on the application. Many different components make up the VLSI chip circuit, ranging from analog and digital to electromechanical and electrochemical. The sponging components inside the chip are accountable for the chip's maximal power dissipation. During switching or active mode operation, IC power is dissipated. The dynamic and standby leakage components are the two main reasons for leakage.

When the gate terminal is deactivated, and no channel is present, the leakage current flows among the source and drain terminal. The drain will float due to the idle gate terminal, and there will be no channel current flows. A channel forms between the drain and source terminals as the gate is turned on via a resistive path, allowing current to flow in the mA range. By correcting the body bias conditions or power-gating, the standby leakage can be made significantly smaller than the active leakage.

Voltage scaling is an excellent way to lessen power dissipation in this case. The voltage scaling disturbs the circuit's switching speed as switching time is inversely associated with supplying voltage. To correct it, systems can use dynamic voltage scaling to accomplish the lowest VDD required while preserving energy for processing.

As per the International Technology Roadmap for Semiconductors (ITRS),[1] total power usage may becontrolled by leakage power dissipation. An important parameter for VLSI circuit designers is the leakage powerdissipation for the new CMOS sizes. Static and dynamic components contribute to CMOS power consumption. When transistors switches, dynamic power is consumed. Dynamic power accounts for 90% or more of total chip power (at 0.18 technologies and above), making it the significant concern for low-power chip designers. As a result, many previously proposed solutions, such as voltage and frequency scaling, were largely aimed at lowering dynamic power. As element size shrinks to 0.09 and 0.065, static power becomes a serious alarm for current and future technology. Power losses in CMOS circuits can occur for a variety of reasons. Different forms of leakage components are depicted in Figure 1.

In leakage power growth,[2] it is mainly due to increased sub-threshold leakage power. The sub-threshold region is the name given to the weak reversal zone. Thecurrent that flows in mid-way between drain and sourceof a MOSFET is called sub-threshold leakage, also, in weak inversion zone

Corresponding Author: Ritesh Sadiwala, Department of Electronics and Communication Engineering, RKDF University, Gandhinagar, Bhopal-462003, Madhya Pradesh, INDIA, e-mail: ritesh14ci@gmail.com

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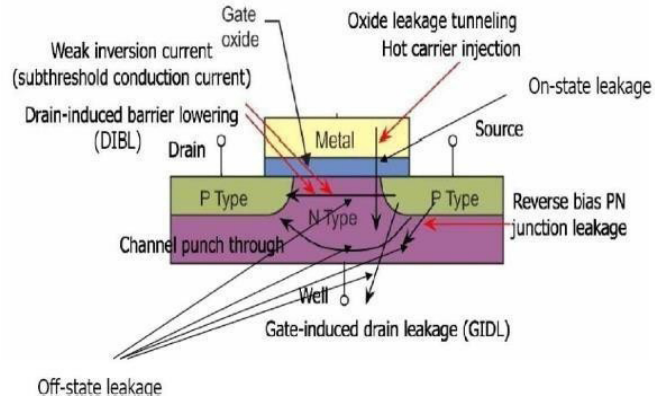

Figure 1: Leakage power components in CMOSThey are:
1. Due to weak inversion current.
2. Gate oxide leakage (Tunneling current)
3. Channel punch Drain leakage

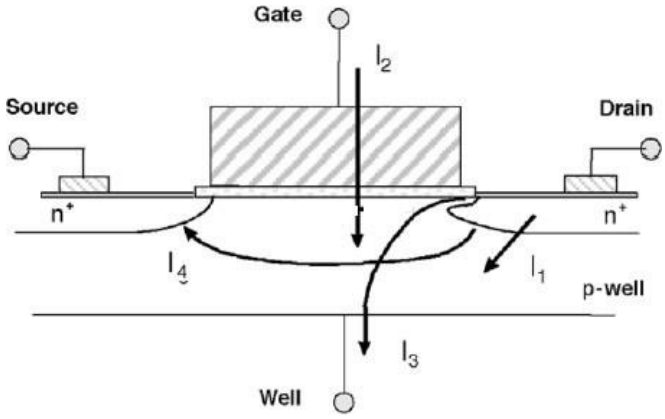

Figure 2: Sub-threshold Leakage currents in MOSFET

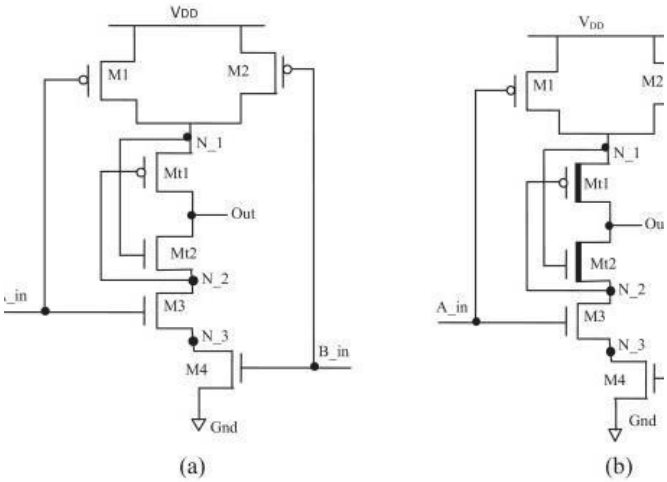

Figure 2: (a) LCT NAND gate and (b) HTLCT based NAND gate.

the transistor is in the sub-threshold region. The threshold and supply voltage are both decreased when the size of a technical feature is reduced. The sub-threshold leakage power increases exponentially as the threshold voltage drops. Next, to improve channel conductivity and performance, the gate oxide, which acts as an insulator between the gate and the channel, should be made as thin as feasible so that the oxide's barrier voltage changes. As a result of the positive gate voltage, some positive charges become trapped in the oxide, due to which current passes through the oxide. The tunneling current is another name for this phenomenon.

The portions of the long-channel devices, such as drain and source, are spaced plenty apart such that their depletion zones have no consequence on the device's potential or field pattern. Thus, the threshold voltage of such devices is unaffected by channel length of drain

bias. Band bending over a considerable amount of a short channel device is influenced by the vertical depletion width of the source and drain, and its potential. Thus, the drain bias influences the threshold voltage and its sub-threshold current of the short channel devices. Drain-Induced Barrier Lowering (DIBL) is the name for these phenomena.

High Threshold Leakage Control Transistor (HTLCT)

To diminish the static leakage power dissipation in the CMOS circuit, the dual threshold is used with delay tradeoffs.[3] A higher threshold voltage transistor in use instead of the self- control series-connected transistor method. Figure 2 shows theleakage control transistor for NAND logic gate with two PMOS M1, M2 connected in parallel structure and two NMOSM3, M4 connected in series structure. With these two transistors Mt1, Mt2 high threshold transistors are connected in PUN and PDN across which the output load capacitor is connected. This transistor can acts as a self-control self-bias transistors. The input Gate terminals of these transistors are connected to the source terminal of each other. One of the transistors among Mt1 and Mt2 operates in a Cut off region. This increases the stack transistor effect between supply and ground rail. This helps to diminish the leakage powerdissipation.

A TG-based Technique forLeakage Optimization

In the Transmission gate (TG) method, a TG is inserted ahead ofa logic circuit which needs protection against the leakage power. The circuit in Figure 2 is an Edge triggered D flip-flop that uses three SR latches to operate. Two latches are triggered by the external D (data) and CLK (clock) inputs. The third latch provides the flip-flop with its outputs. When CLK = 0, the output latch's S and R inputs arekept at the logic1 level. As a result, the output rests in its current state. The value of D can be 0 or 1.

Supply Voltage Scaling

In MOSFETs, the supply voltage VDD is proportional to the static and dynamic power dissipation. As a result, scaling the supply voltage is the most efficient way to shrink power dissipation.

$$P_{dynamic} = \alpha C_L V_{DD}^2 f_{CLK} \text{ and}$$
$$P_{static} = V_{DD} I_{ds} \quad (1)$$

Where,

α is the constant

C_L is the total load capacitance

V_{DD} is supply voltage

f_{CLK} is the clock frequency

The switching delay of MOSFET is:

$$T = KC_L/\beta V_{DD} \text{ and } \beta = \mu \text{ Cox } W/L \quad (2)$$

Where,

β is MOSFET Gain Cox is oxide capacitance

W/L is the ratio of MOSFET Channel width and length. Because the switching delay is inversely related to the supply voltage, voltage scaling for reduced powerdissipation will increase switching delay.

When CLK converts 1, D becomes 0 and R becomes 0. This sets the flipflop to its reset state, resulting in Q = 0 as shown in Fig. 3. Because Q is 0, if the D input changes while CLK = 1, terminal R remains at 0.R goes to 1 when the clockreturns to 0, putting the output latch in the quiescent stateand not modifying the output.[6] Similarly, when CLK goesfrom 0 to 1, D equals 1 and S equals 0.

This changes the circuit to the set state, causing in

Q = 1. The transition from 0 to 1 and nothing else.[7] Itmakes a positive conversion; the value of D is moved to

Q. When the CLK is in the steady logic-1 level or the logic-0 level, a negative clock transition (i.e., from 1 to0) does not affect the output, nor do fluctuations in D when CLK is in either logic level.

Mtcmos Technique

High-threshold devices are utilized as sleep transistors in multi-threshold voltage CMOS circuits (MTCMOS), although the logic can be implemented using low- threshold devices as given in Figure 4.

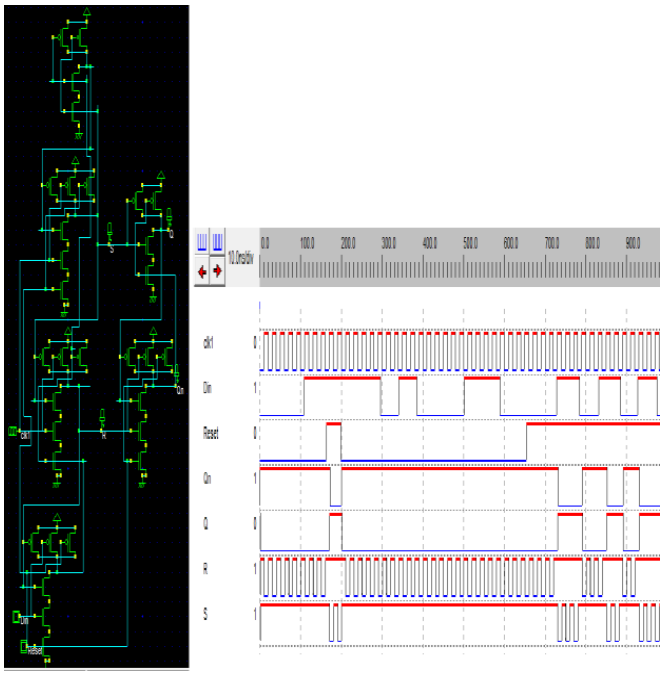

Figure 3: Transmission gate Base Flip Flop.

In practice, one sleep transistor is engaged per gate, althoughincreasing granularities necessitate rarer but larger sleep transistors. NMOS sleep transistors are typically used because their input resistance is lesser than that of PMOS at the same width; thus, NMOS has a size benefit over PMOS. However, there are some drawbacks associated with this strategy in terms of area. The gates' transistors have a low threshold voltage, and the gate is coupled to the ground via an NMOS gating transistor with a high threshold voltage. The logical function of gating transistor and a sleep transistor is comparable. Due to this, reverse conduction routes reduces the noise margin and, in the worst-case scenario, cause the gate to fail. Furthermore, performance improves as high threshold transistors are connected in series with all switchingcurrent channels.

The Dual VT approach uses transistors with twodistinct threshold voltages, is a version of the MTCMOS technique.[4] Low-threshold transistors are utilized for critical route gates, while high-threshold transistors are employed for non-critical path gates. Extra mask layers for each threshold voltage value are required in both MTCMOS and Dual VT to fabricate transistors selectively according to their allotted threshold voltage standards. This complicates the fabrication process.

Body Bias Technique:

The body voltage can be altered in bulk silicon devices to change the threshold voltage. Different NMOS transistors

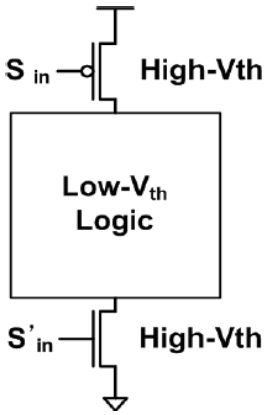

Figure 4: Multi-Threshold CMOS (MTCMOS)

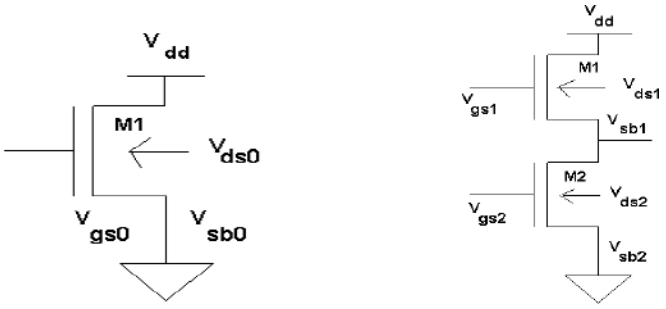

Figure 5: (i) Single Transistor (ii) Stacked transistor

cannot share the same well if their body biases are applied separately, necessitating the use of triple well technology. As SOI devices are logically split, altering its bias is easy in moderately depleted cases. Consider the completely depleted double gate SOI, in which the surface potentials of the front and back gates are inextricably coupled. To adjust the threshold voltage, the back gate voltage can be biased. This technique aims to use post-silicon tweaking to fulfill the delay and power restrictions in each die. The body bias technique is taken to increase performance in slow and less leaky devices forward, while reverse body bias is used to reduce leakage in fast and highly leaky devices. Thus, the impact of parameter fluctuations is minimized by post-silicon adjustment, which reduces the impact of process variability while also enhancing total yield.

Proposed Leakage Reduction Stack Transistor Methodology

Stacks of books (Self Reverse Bias)

When more than one transistor in a stack of series linked transistors is turned off, the sub-threshold leakagecurrent flowing through the stack decreases. The "stacking effect" is the name for this effect. Consider the stacking effect as a two-input NAND gate as shown in Fig. 5. When both inputs M1 and M2 are turned off, the voltage at the in-between node (VM) is positive due to the small drain current. At the intermediate node, there are three positivepotential controls. The gate to source voltage of M1 (Vgs1) converts negative as a result of the positive source potential VM, and the sub-threshold current decreases significantly.

1) M1's body to source potential (Vbs1) becomes negative when VM > 0, causing M1's threshold voltage (larger body effect) to rise, lowering sub-threshold leakage.
2) M1's drain to source potential (Vds1) declines as VM
   > 0, resulting in a rise in M1's threshold voltage (less DIBL) and hence a reduction in sub-threshold leakage.

A two-transistor stack has a leakage that is lower than a single transistor.

Conclusion

The logic design with static CMOS with low voltage low power circuits is often slow and cannot be used in high-performance circuits. Thus the use of dynamic CMOS logicis the better remedy for high-performance less area design circuits. But it has increased power dissipation. The paper gives a strategy for minimizing the parameters like dynamic power, area and leakage of application-specific integrated circuits without sacrificing performance. With its advantagesof smaller size and low power dissipation, the hybrid dynamic and static CMOS circuit will solve the shortcomings.

References

[1] NiranjanKulkarni, Jinghua Yang, Jae- Sun Seo, SarmaVrudhula (2016, September) "Reducing Power, Leakage, and Area of Standard- Cell ASICs Using Threshold Logic Flip-Flops" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, 24(9), 2873 -2886.

[2] Preeti Verma, Ajay K. Sharma, VinayShankarPandey, Arti Noor, AnandTanwara (2016, September) “Estimation of leakage power and delay in CMOS circuits using parametric variation”, 8, 760-763.

[3] Ing-Chao Lin, Kuan-Hui Li, Chia-Hao Lin, and Kai- Chiang Wu. (2014, September), " NBTI and Leakage Reduction Using ILP-Based Approach" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, 22(9), 2034-2038.

[4] Simone Balati, Stefano Ambrogio, and Danıelelelmını, (2015, June),"Normally off Logic circuits Based on Resistive Switches” IEEE Transactions, Electron Devices, 62(6), pp no.1839

[5] Mathieu Luisier and Olaf Schenk, (2013, October), "Gate-Stack Engineering in n-Type Ultrascaled Si Nanowire Field-Effect Transistors", IEEE Transactions On Electron Devices, 60(10);3325-3329.

[6] MehrzadNejat, BijanAlizadeh, and Ali Afzali-Kusha, (2015, November), "Dynamic Flip-Flop Conversion: A Time-Borrowing Method for Performance Improvement of Low- Power Digital Circuits Prone to Variations" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, 23(11), 2724-2727.

[7] A. Parvathi Karthica (2013, April), "Power Efficient Synchronous Counter Using Transmission- Gate Based Master-Slave Flip-Flop With Modified Logical Effort Optimization", 7th International Conference on Electronics and Communication Engineering (ECE) ,Bangalore.