RESEARCH ARTICLE

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Speed Optimization of Image Processing Application using FPGA Based Multi-Processor System on Chip

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ABSTRACT

Speed optimized embedded devices with low power consumption are demand of today's world. Now a day's, these devices are used in complex application such as cryptographic algorithm, digital signal processing, image processing etc. Multiprocessor based systems are faster as compared with single processor based systems because it performs multiple tasks in parallel fashion. Hence, Field Programmable Gate Array (FPGA) based Multi-Processor System on Chip (MPSoC) can be an efficient option for speed optimization.

This paper presents work on speed optimization of image processing application in hardware setting using efficient and fast FPGA based MPSoC. The multiprocessor environment was developed using MicroBlaze soft-core processor with Xilix sparten-3e starter board. Edge detection being fundamental need of image processing, hence SOBEL edge detection algorithm was implemented on single processor based environment as well as on developed MPSoC. To estimate the actual time of processing, software profiling was done which showed FPGA based MPSoC reduces overhead on master processor & hence improvement in computational speed was observed as compared to single processor environment.

Keywords: MPSoC, FPGA, MICRO-BLAZE, SOBEL, Edge Detection, Soft-Core Processor.

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INTRODUCTION

Today's high-performance computing applications like image processing, Audio/Video signal processing, cryptography application demands high speed & low power consumption. Such applications need faster, flexible, configurable & better energy efficiency embedded systems. FPGA based soft core processors are advantageous for designing such embedded system as they are flexible, can be customized for any application, technology independent.

Software implementation is not much useful but real time hardware system on chip is more efficient for image processing application [1], [2]. Efficient hardware of any image processing application is possible in FPGA, FPGA memory can hold image processing algorithm to process image of any size [3], [4]. Implementation time can be improved by using software for generating hardware description language (HDL) from a high-level MATLAB description for particular algorithm [5], [6].

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MPSoC architecture is an efficient option for speed optimization because it uses multiple processors for implementing any application [7], [8]. Real time processor, dedicated graphics core, programmable logic all are in single chip, which makes MPSoC as a high-performance processing system. Hence real time hardware simulation is possible using MPSoC based embedded system [9].

MPSoC is basically, many processor memory modules (PMM) available on single silicon chip with separate cache memory available for each processing element which are connected together by communication bus. [10].

The development phase of MPSoC environment includes following major steps:

1. Platform configuration
2. Code generation
3. Application development
4. Application mapping on to the platform
5. Debugging

According to the system architecture model, there are two types of MPSoC, Homogeneous and Heterogeneous. In the Homogeneous MPSoC, processors are of similar architecture but in Heterogeneous MPSoC same platform have different processor architectures.

In the proposed work, an environment for MPSoC using Micro-blaze soft core processor is developed. After developing the complete system, it is implemented on FPGA, Sparten-3eStarter board. Sobel Edge detection algorithm is implemented on MPSoC as well as Single processor based system on chip. Time analysis is performed for validation of results & comparison presented for both the environments.

MULTI-PROCESSORS SYSTEM ON CHIP

Multi-Processor

Two or more processor on a single chip which are used to implement any application are speed optimized [11]. Because in multiprocessor environment, there are many processor which divides task in parallel fashion, master processor is main processor and slave processor perform many tasks hence overheads on master reduces. Multiprocessor based environment can be developed on soft core processor.

Microblaze Soft-Core Processor

Internal structure of Xilinx Microblaze soft-core processor is shown in Figure 1[12].

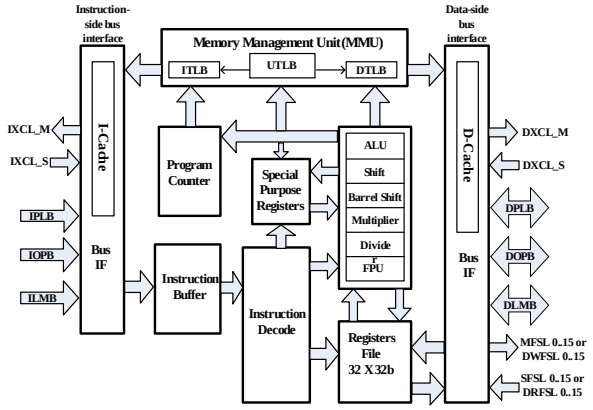

Figure 1: Microblaze Soft-Core Processor Internal Structure

MicroBlaze processor has different buses like FSL (Fast Simplex Link, PLB (Processor Local Bus) Bridge. Eight input & eight output FSL interfaces are available in MicroBlaze Processor. FSL Bus signal in MicroBlaze processor is shown in figure 2.

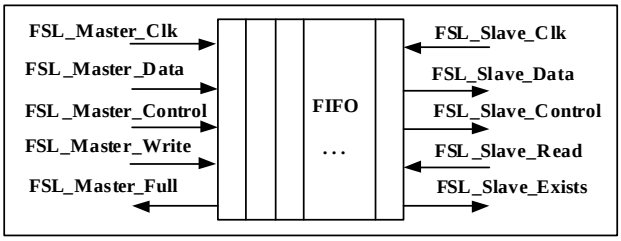

Figure 2: FSL bus signa

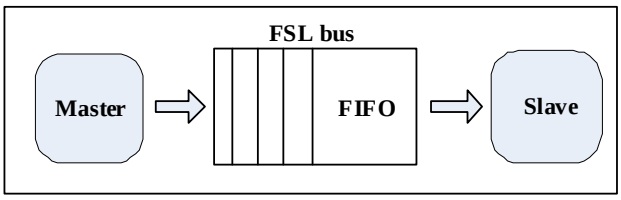

Figure 3: FSL interlink

FSL_M represents for master processor end & FSL_S represents for slave processor end. Set of transfer macros putfsl (value, port no.) and getfsl (value, port no.) are used to send data to other processor by master. Value means data to be over FSL & FSL port used for communication is represented by port number. Figure 3 shows FSL interlink between master and slave processor. Basic embedded design flow is shown in figure 4 [13].

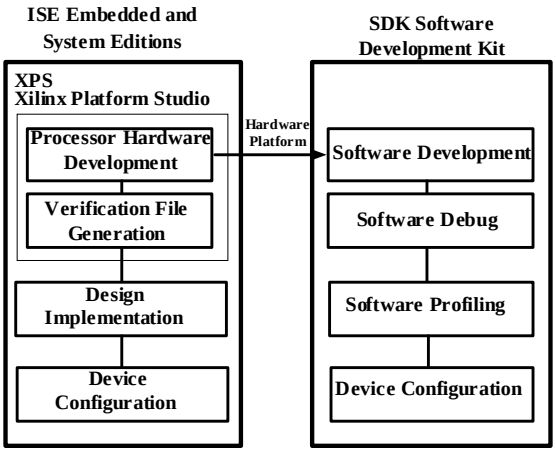

Figure 4: Basic embedded design flow

IMAGE PROCESSING APPLICATION

Edge Detection

Edge in any image means sharp changes in intensity of an image or a set of connected pixels that form a boundary between two disjoint regions. Edge detection means detection of outline, sharp changes or identifying any object [14]. Edge detection is important need of computer vision as it detects boundaries of any object.[15] Edge detection is fundamental need of image processing which is important in medical application like X-Ray, Tumor detection, satellite image, robotics vision like electric car, driverless car, face reorganization, figure print detection etc. Many researches show that, software implementation is not efficient for real time applications [16], [17]. Hence its hardware implementation is more efficient for real time applications [18], [19].

The Sobel edge detection method is simple & it provides approximation to gradient magnitude. Edges and their orientation can also be detected by Sobel Operator. Hence sobel edge detection is preferred.

Sobel edge detection algorithm detects edges of image very effective [20, 21, and 22]. Consider I is any image & $[I]_{3x3}$ is its sub-window, Z5 is pixel of interest, & Z1, Z2, Z3, Z4, Z6, Z7, Z8, Z9 are neighboring pixel. Sub-window of image $[I]_{3x3}$ is given in equation 1.

$$[I]_{3X3} = \begin{pmatrix} Z_1 & Z_2 & Z_3 \\ Z_4 & Z_5 & Z_6 \\ Z_7 & Z_8 & Z_9 \end{pmatrix} \quad (1)$$

$$\text{Horizontal Mask} = \begin{pmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{pmatrix} \quad (2)$$

$$\text{Vertical Mask} = \begin{pmatrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{pmatrix} \quad (3)$$

Edges are detected by scanning image with sobel mask from left to right by horizontal mask & top to bottom by vertical mask as shown in figure 5. Consider Gradient in horizontal is Gh & vertical direction is Gv.

$$Gh = \begin{pmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{pmatrix} * I \quad (4)$$

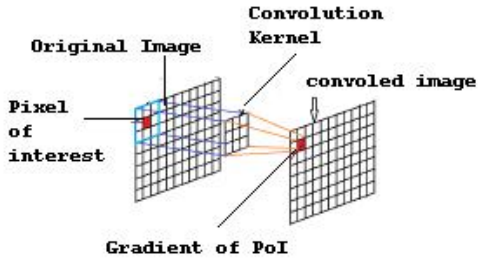

Figure 5: Scanning of an Image using sobel mask

$$Gv = \begin{pmatrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{pmatrix} * I \quad (5)$$

Where, I is an original image.

Edge strength is equal to magnitude of gradient which is given by equation 6 or equation 7.

$$G = \sqrt[2]{Gh^2 + Gv^2} \quad (6)$$

$$G = |Gh| + |Gv| \quad (7)$$

& edge direction is given by equation 8.

$$\theta = \tan^{-1}\left(\frac{Gv}{Gh}\right) \quad (8)$$

PROPOSED DESIGN APPROACH

According to proposed methodology, MPSoC environment is developed on MicroBlaze soft-core processor & Sobel edge detection algorithm is

implemented on it. To estimate the actual time of processing, software profiling was done. To validate results, same algorithm implemented on single processor based environment & software profiling result of single processor based environment is compared with software profiling result of MPSoC environment. Proposed implementation flow shown in figure 6.

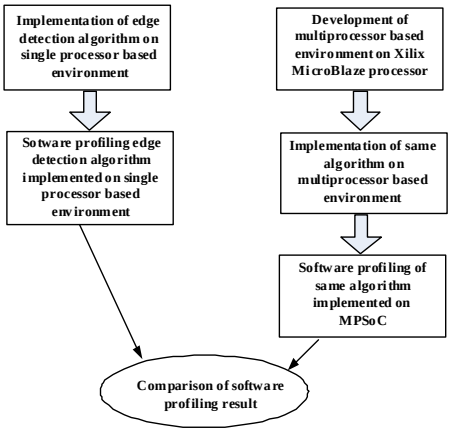

Figure 6: Proposed flow of implementation

VHDL Simulation for Sobel Edge Detection Algorithm: VHDL is high level descriptive language which describes any digital logic circuit in three ways: structural, behavioral & dataflow [23]. VHDL implementation of sobel edge detection algorithm is efficient approach [24], [25]. HDL Sobel edge detection algorithm is simulated on Xilinx EDK 13.1. Simulation result for sobel operator is shown in figure 7.

Figure 7: . Simulation result of Sobel operator

Implementation of Sobel Algorithm on Single Processor : Sobel algorithm is implemented on single processor based environment using MicroBlaze soft-core processor on sparten 3e, FPGA board. Xilinx EDK tool based system is developed using serial communication through UART (Universal Asynchronous Receiver Transmitter) as shown in figure 8.

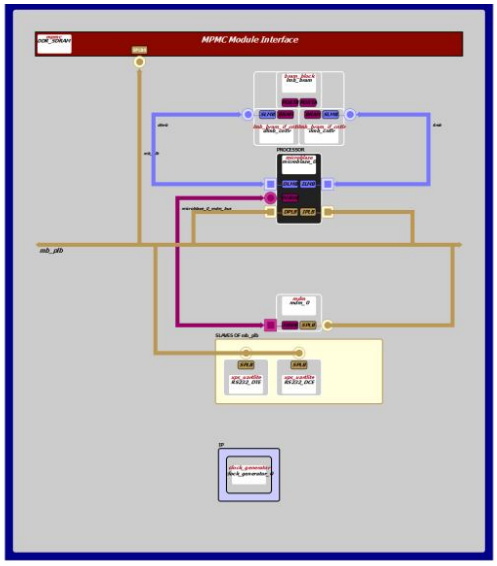

Figure 8: Single processor environment implemented in EDK

Implementation OD Sobel Algorithm on Single Processor : Using ilix ise13.1 based EDK tool duel MicroBlaze based system is developed as shown in figure 9. On a dual processor system, the same algorithm was implemented and both processes are made to work in parallel.

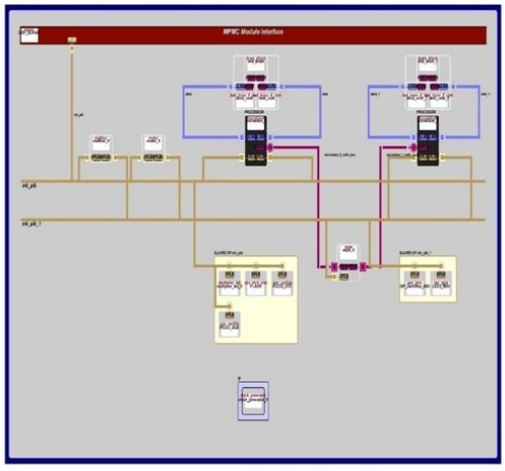

Figure 9: Duel-processor environment implemented in EDK

RESULT

For testing edge detection algorithm, original image of SBJITMR shown in figure 10 (a) is used. Figure 10 (b) is grayscale image of SBJITMR. MATLAB simulation result is shown in figure 10 (c). MATLAB simulation of Sobel edge detection algorithm takes 496.22µsec. same algorithm is implemented on FPGA using single processor and multiprocessor based environment & results are shown in figure 10(d) & 10(e) respectively.

Figure 10 a. : Original Image SBJITMR

Figure 10 b. : Grayscale image SBJITMR

Figure 10 c. : Sobel Edge Detection SBJITMR using matlab simulation

Figure 10 d. : Sobel Edge Detection SBJITMR on Single Processor

Figure 10 e. : Sobel Edge Detection SBJITMR on Multiprocessor

Software profiling is done for time analysis. Software profiling results for single processor as well as multiprocessor based environment is shown in figure 11 & 12 respectively. Hardware implementation of same algorithm on single processor based environment takes 11.53 µsec (1.278 µsec for image display & total 10.246 µsec for edge detection). Hardware simulations on multiprocessor based environment takes 4.79 µsec (1.28 µsec for image display & 3.522 µsec for edge detection).

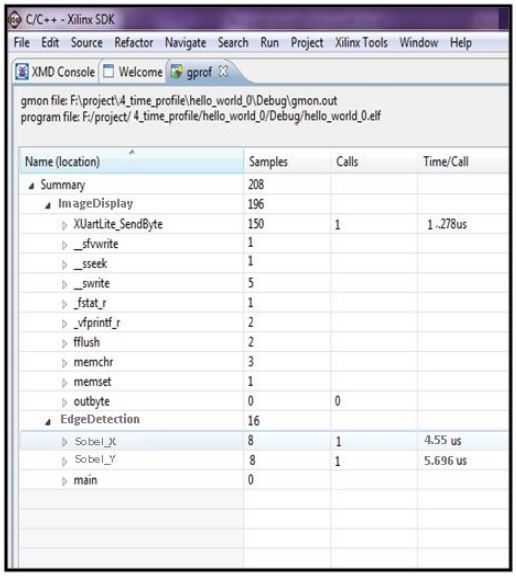

Figure 11: Profiling result for single processor based enviornment

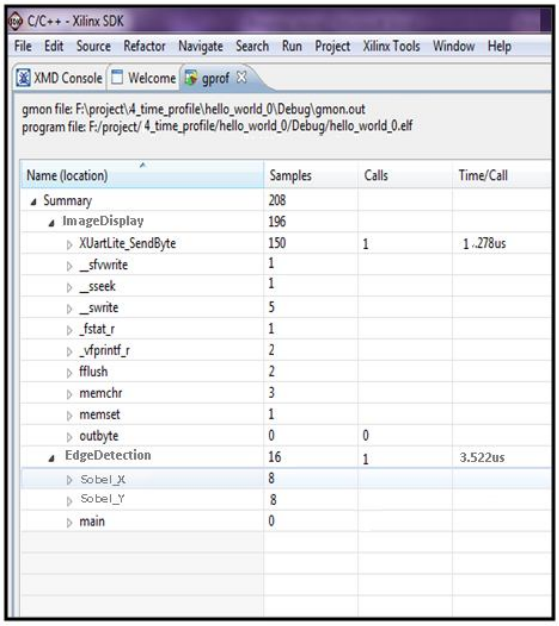

Figure 12: Profiling result for multiprocessor based environment

Table-1: Comparison of Processing Time

Sr. No.	Implemented Environment	Processing time for edge detection
1	Software Environment through MATLAB simulation with SOBEL edge detection algorithm	**496.22 µsec.**
2	Hardware Environment through Single Processor based FPGA with SOBEL edge detection algorithm	**11.53 µsec.**
3	Hardware Environment through FPGA based MPSoC with SOBEL edge detection algorithm (proposed)	**4.79 µsec.**

From above results we can conclude that multiprocessor environment can save 58.45% of processing time. MPSoC based system is speed optimized as compared to single processor based system.

CONCLUSION

Multiprocessor based environment using MicroBlaze soft-core processor divides certain task into different modules and perform it in parallel way so that computation speed is faster. Therefore, multiprocessor based environment was created using MicroBlaze Soft-Core Processor and SOBEL edge detection algorithm was implemented in it.

Earlier researchers have implemented their work in single processor environment. The proposed work was carried out with multi-processor environment and it validates that the multi processor environment is faster for image processing applications with SOBEL edge detection algorithm and hence can be effectively used for image processing applications.

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