RESEARCH ARTICLE

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Reconfigurable Successive Approximation Register ADC and SAR-Assisted Pipeline ADC

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ABSTRACT

The paper proposes an analog to digital converter (ADC) which is reconfigurable and it consists of successive approximation register (SAR) ADC and SAR-Assisted pipeline ADC that can improve the resolution and conversion time based on the application. This reconfigurable ADC is designed to obtain an 8-bit resolution with low conversion time, a 16-bit (8-bit + 8-bit) resolution in pipeline mode with optimum conversion time and 16-bit (8-bit + 8-bit) resolution in sub ranging mode with more conversion time using exsisting components. This proposed ADC behaves as 8-bit SAR ADC, 16-bit (8-bit + 8-bit) two stage SAR-Assisted pipeline ADC and 16-bit (8-bit + 8-bit) two step sub-ranging ADC. The reconfigurability is obtained using control signals. This circuit has been designed and simulated in NI Multisim 14.0, and the results are presented in the paper.

Keywords: Reconfigurable, SAR ADC, SAR-Assisted pipeline ADC.

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INTRODUCTION

Reconfigurable ADCs are programmed to achieve conversion with optimum ADC parameters like number of bits, conversion time and etc. Such ADCs are required for different communication systems [1], signal processing and wireless sensor networks [2]. Several methods are used to reconfigure various types of ADCs such as flash, SAR, pipeline, single slope, delta-sigma signal ADCs etc. Reconfigurable ADCs are being used in various applications such as the bio instrumentation [3] biomedical sensors [4] wireless personal area network application [5] sensor applications [2]. It is difficult to achieve high resolution high speed low power at the same time in conventional ADCs. A tradeoff must be made in order to get these features. Hence ADCs are reconfigured to overcome these drawbacks. Reconfigurable ADCs are power budgeting [3], it can change the operable resolution and sampling rate [6]. For 8 to16-bit resolution and sample frequency around 5MHz applications, SAR ADC is used [7] which is advantageous due to low power dissipation, high accuracy and low latency [8]. The SAR ADC has been used often for data processing which is part of processing industrial systems, and also optical communication systems [9]. The conversion time of SAR ADC increases due to increase in resolution. So, to accomplish different applications of SAR ADC with high resolution and low conversion time this ADC has been reconfigured in this proposed method.

Figure 1 shows general diagram of a basic SAR ADC. It includes comparator, sample and hold circuit, SAR logic, DAC and control circuit. The analog input

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voltage (Vin) is held constant by the sample-and-hold circuit. The analog voltage is then digitized using a binary search algorithm. After receiving start of conversion (SOC) command the input signal is held constant and SAR logic circuit sets the MSB bit to 1 while all other bits are set to 0. And this SAR logic output which acts as an input to DAC sets its output equal to Vref/2. This DAC output is compared with the input signal.

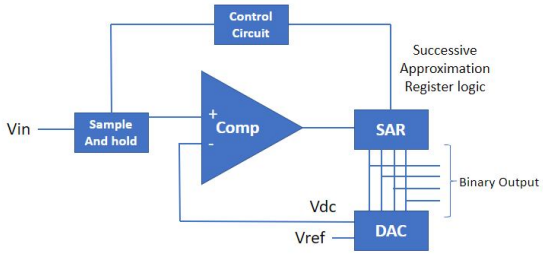

Figure 1: General block diagram of SAR ADC

The output of comparator depends upon the Vin and the DAC output. If DAC output is less than Vin then output of comparator goes high and SAR register sets the MSB bit input of DAC at 1.

On the contrary if DAC output is greater than Vin, then the output of comparator goes logic low and the SAR register resets MSB bit input of DAC to 0. The SAR circuit then shifts to the subsequent lower bit, and the process is repeated until remaining digital data is decided. Then the final digital data is present in the register after deciding all the bits and the coming analog input is sampled and is available for conversion. In this paper, reconfigurable SAR, SAR-Assisted pipeline ADC and subranging ADC has been designed and simulated using National Instruments MultiSim 14.0.

PROPOSED DESIGN

Figure 2 represents the proposed design of a reconfigurable SAR ADC which is varied as 8-bit SAR ADC with lower conversion time, 16-bit SAR-Assisted pipeline ADC with optimum conversion time and 16-bit two step sub ranging ADC with higher conversion time. It consists of two 8-bit SAR ADCs, subtractor, 16-bit DAC, residue amplifier (Gain-256), sample and hold circuitry and multiplexers.

The selection of different modes is done by the control circuitry as shown in Table 1.

Table-1 : Control Signal

A	B	Mode Selected
0	0	8-bit SAR
0	1	16-bit SAR-Assisted Pipeline
1	0	16-bit Subranging

If the control signal A=0, B=0 is selected then the reconfigurable ADC behaves as 8-bit SAR ADC. The 8-bit SAR ADC1 converts the input signal into 8-bit digital output for 8-bit resolution. This 8-bit SAR ADC1 output is then given to the data selector as d0-d7 and 8-bit SAR ADC 2 output d8-d15 is at logic 0. This d0-d15 data is brought on the same data line by using multiplexers and b0-b7 8 MSB bits are final 8-bit data while b8-b15 are at logic 0. The conversion time of this 8-bit SAR ADC is T.

If the control signal A=0, B=1 is selected then the reconfigurable ADC behaves as 16-bit SAR-Assisted pipeline ADC. In pipeline mode with 16-bit resolution, d0-d7 8 MSB bits are acquired using 8-bit SAR ADC1. This digital output is then fed to a DAC having 16-bit resolution. The subtraction of analog signal of DAC output and an input voltage is done to obtain the remainder called residue which is amplified by the residue amplifier with a gain of 256. The residue output is held constant by the sample and hold circuit till the completion of LSB 8-bit conversion. During LSB 8-bit (d8-d15) conversion of sample1 by SAR ADC2, the 8-bit SAR ADC1 completes the conversion of the 8 MSB bits of sample2.

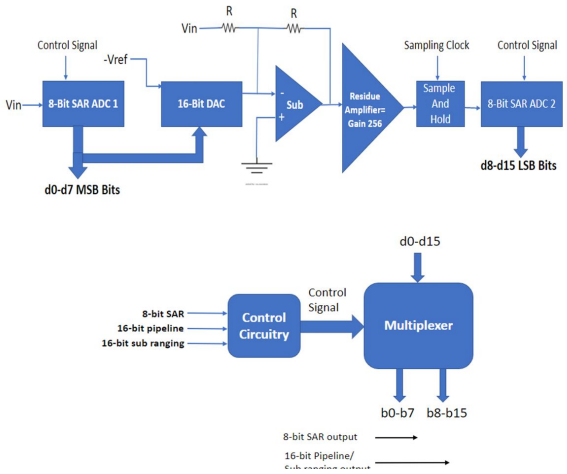

Figure 2: Block Diagram of Proposed ADC

The LSB 8-bits are obtained as d8-d15. In pipeline mode the SOC is given to MSB 8-bit SAR ADC1 and LSB 8-bit SAR ADC2 simultaneously. The data d0-d15

is brought on the same data line by the multiplexer whose 16-bit output is b0-b15. This is how it operates in pipeline mode which reduces the conversion time significantly and it is equal to T + 16-bit DAC settling time + two op-amp settling time.

The timing diagram of the 16-bit SAR-Assisted pipeline ADC is shown in Figure 3. During the positive half of the first clock the MSB 8-bits of sample1 are obtained and during its negative half the output for LSB 8-bits of sample1 are obtained and parallelly the MSB 8-bits of sample2 are obtained and this continues. For the first clock cycle the positive half is doing only one conversion therefore there is one clock delay. From the second clock cycle two conversions are done simultaneously for the positive as well as the negative half hence the conversion time is reduced significantly.

If the control signal A=1, B=0 is selected then the reconfigurable ADC behaves as a 16-bit two step subranging ADC. In subranging mode with 16-bit resolution, the d0-d7 8-MSB bits are achieved using 8-bit SAR ADC1. This digital output is then fed to DAC (16-bit). The subtraction of analog signal of DAC output and an input voltage is done to obtain the remainder called residue which is amplified by the residue amplifier with a gain of 256.

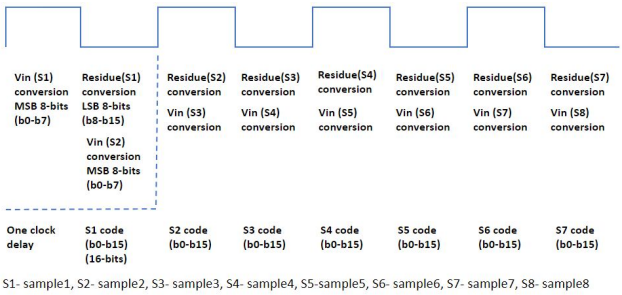

Figure 3: Timing diagram of SAR-Assisted Pipeline ADC

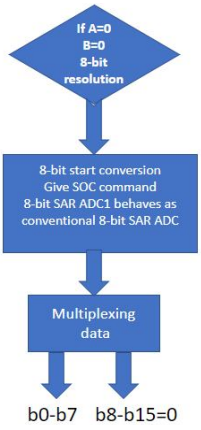

Figure 4: 8-bit SAR ADC Conversion

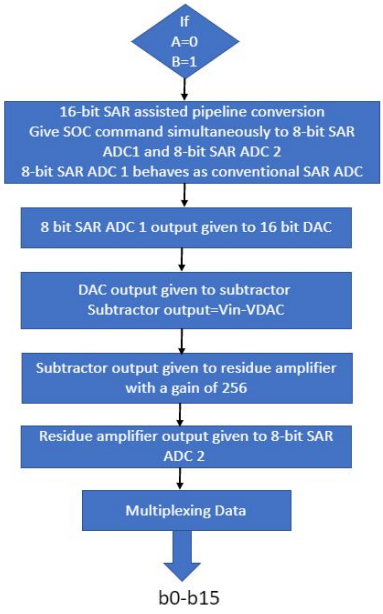

Figure 5: 16-bit SAR-Assisted pipeline ADC conversion

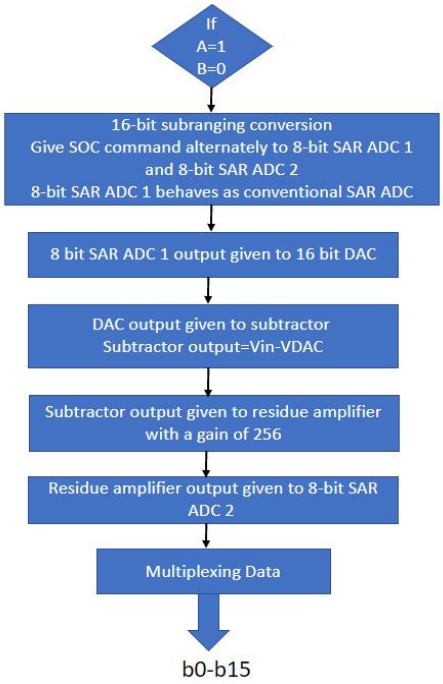

Figure 6: 16-bit subranging ADC conversion

The residue output is held constant by the sample and hold circuit till the completion of LSB 8-bit conversion. The LSB 8-bits are obtained as d8-d15. In subranging mode, the SOC is given to MSB 8-bit SAR ADC 1 and LSB 8-bit SAR ADC2 alternately. The data d0-d15 is brought on the same data line by the multiplexer whose 16-bit output is b0-b15. After completion of first sample conversion this ADC is ready to accept the new sample for conversion. This is how it operates in

subranging mode whose conversion time is more and it is equal to 2T + 16-bit DAC settling time + two op-amp settling time. Figure 4, Figure 5 and Figure 6 shows the flowchart for the process of conversion of 8-bit SAR ADC ,16-bit SAR-Assisted pipeline ADC and 16-bit two stage subranging ADC.

RESULTS

The proposed design has been validated using a ramp signal as an input for resolution such as 8-bit and 16-bit. The validated data is shown in the table where b0 is MSB and b7 is LSB for 8-bit conversion and b0 is MSB and b15 is LSB for 16-bit conversion.

Table-2: 8-Bit Sar Mode

Vin (mV)	b0 (MSB)	b1	b2	b3	b4	b5	b6	b7 (LSB)	b8	b9	b10	b11	b12	b13	b14	b15
40	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
80	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
120	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
160	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Table-3 : 16-bit SAR-Assisted pipeline mode

Vin	b0 (MSB)	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11	b12	b13	b14	b15 (LSB)
160uV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
320uV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
480uV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
640uV	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Table-4 : 16-bit SAR subranging mode

Vin	b0 (MSB)	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11	b12	b13	b14	b15 (LSB)
160uV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
320uV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
480uV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
640uV	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

CONCLUSION

NI Multisim 14.0 is used for design and simulation of the reconfigurable ADC. It has been validated for resolution such as 8-bit and 16-bit by giving an input using a counter with a step size of 40mV for 8-bit conversion and 153uV for 16-bit conversion. Table II, Table III and Table IV indicates the validation result for sample data.

Further improvement in the resolution is possible by modifying the circuit. This ADC will prove itself useful in a variety of electronics and communication field-based applications. So, a single ADC can be reconfigured to give 8 bits with minimum conversion time, 16-bit subranging with higher conversion time and 16-bit pipeline optimum conversion time.

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