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Analysis of Vedic Multiplier for Conventional CMOS & Complementary Pass Transistor Logic (CPL) Logics

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ABSTRACT

In this work we have designed and analyzed Vedic Multiplier for conventional CMOS and Complementary Pass Transistor Logic (CPL). Vedic Multiplier is designed for 4-bit & 8-bit using conventional CMOS gates and CPL gates. Their Speed, Area and Power is analyzed and compared. The design is implemented using HSPICE for 180nm Technology.

Keywords: Vedic Multiplier, CMOS, Adder, Ripple Carry Adder, Complementary Pass Transistor Logic(CPL).

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INTRODUCTION

Multipliers play vital and important role in many of Digital Signal Process- ing (DSP) and various different applications. Multiplication is mathematical operation in which the number is repeatedly added to itself for the specified number of times. Multipliers take more time and area than any other arithmetic operations. Digital Signal Processing (DSP) applications uses Multipliers in performing various operations in convolution of signals, filters, performing (FFT) Fast Fourier Transform and in microprocessors Arithmetic & Logic Unit (ALU) [1-13].

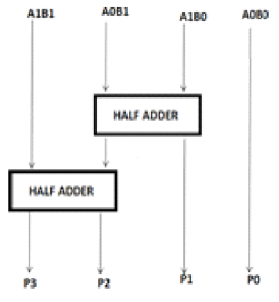

Figure 1: 2-Bit x 2-Bit Vedic Multiplier

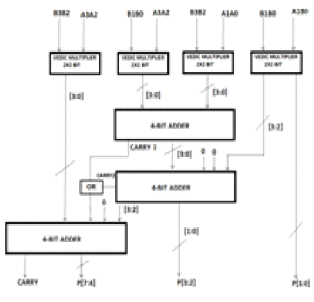

Figure 2: 4-Bit x 4-Bit Vedic Multiplier

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VEDIC MULTIPLIER

Vedic Mathematics is ancient Indian Vedic system of Mathematics. Indian Vedic sutras are used in Vedic Multiplier for improving multiplier speed. This ancient system of Vedic Maths is developed based on the sixteen Vedic Sutras which describe the natural way of solving mathematical problems. Chidgupkar P.D and Karad M.T [14-15] has proposed vedic algorithms usage in multiplication process of 8085 & 8086 microprocessors and there was appreciable time saving in the process. An NxN- bit parallel overlay multiplier architecture was proposed Thapliyal H and Srinivas M.B [16] for the

high speed (DSP) Digital Signal Processing applications. Vedic Multipliers is used in applications which require low power & high speed Rabaey J., Chandrakasan A et al. [17] . Vedic Multiplier complexity is less as compared with booth multiplier architecture. Vedic multiplier hardware uses less no of transistors. Therefore, Vedic multiplier has more advantages in the terms of area, delay, power and complexity. In this Vedic Multiplier Urdhva - Tiryagbhyam Sutra technique is used. Ramesh Pushpangadana, Vineeth Sukumarana et al. [26] has implemented 8x8 and 16x16 vedic multiplier and Booth wallace tree multilier and vedic multilier has shown that vedic multiplier is much faster than Booth wallace tree multiplier. The vedic multiplier was implemented using reversible gates by Gowthami. P and R.V.S. Satyanarayana [11] and had got an optimized structure for 2x2 multiplier. M. Akila, & C. Gowribala et al. [27] implemented vedic multiplier using modified Carry Select Adder has shown an increase in speed. Sheetal N. Gadakh, Amitkumar Khade [28] has implemented vedic multiplier implemented using modified Carry Save Adder has shown 33.26% reduction in delay as compared to Ripple Carry Adder(RCA) and Carry Select Adder(CSA). The Figure 1 shows 2-Bit X 2- Bit Vedic Multiplier. The Figure 2 shows 4-Bit X 4-Bit Vedic Multiplier. The Figure 3 shows 8-Bit X 8-Bit Vedic Multiplier.

CMOS (COMPLEMENTARY MOS) LOGIC

CMOS Logic is most mainstream MOSFET innovation. CMOS innovation has the fundamental favorable position of a lot little power dissipation and further more CMOS has no static power dissipation. The power dissipation happens only when there is switching. This enables us to incorporate more CMOS on IC than bipolar or NMOS transistors and bringing about better execution.

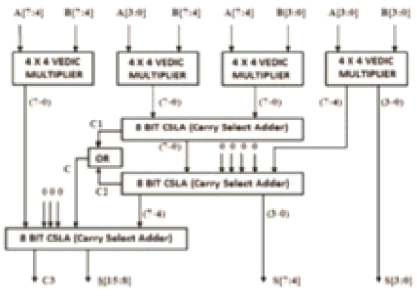

Figure 3: 8-Bit X 8-Bit Vedic Multiplier

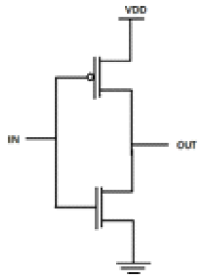

Figure 4 : CMOS Inverter Circuit

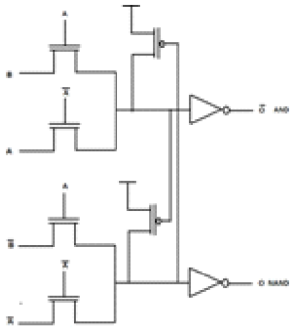

Figure 5 : CPL AND& NAND gate circuit

Any logic functions in CMOS technology are implemented using NMOS transistors and PMOS transistors. An input signal applied turns on transistor of one type and while turns off transistor of other type. Simple switches are used in CMOS design and pull up resistor are not needed.

Pull up and pull down networks are there in CMOS logic. Pull up network is between power supply and output, pull down network is placed between output and the ground. The pull-up network has only PMOS transistors in between output and supply voltage. Inputs are connected to both the transistors PMOS and NMOS and due to input either the PMOS transistor is switched ON and NMOS transistor is switched OFF and its vice versa.

CMOS inverter circuit is as shown in the Fig. 4 when the IN input is low this makes the PMOS transistor to switched on and makes the NMOS transistor to off and therefore the output OUT is logic high. Similarly, when the IN input is made high the PMOS switched is turned OFF and the NMOS transistor is switched ON and therefore the output OUT is logic low.

CPL (COMPLEMENTARY PASS TRANSISTOR LOGIC)

In CPL(Complementary Pass Transistor Logic) implementation only the NMOS transistors are used for logic realizations. CPL(Complementary Pass Tran- sistor Logic) consists of both normal and complementary inputs & out- puts. The logic functionality is implemented using network consisting of only NMOS pass transistor and the inverters at output implemented using CMOS. CPL(Complementary Pass Transistor Logic) requires both the inputs Inverted & non-inverted that are required to drive gates in pass transistor network. We can use PMOS transistors instead of CMOS inverters. Since the output of pass transistor is less than power supply voltage and this is needed to be pulled up it is done by using CMOS inverter at the output or PMOS Latches. By The usage CMOS inverter/ PMOS latches at the output assure output to have better voltage swing similar to input signal and the switching speed is high. Input voltage levels of CPL (Complementary Pass Transistor Logic) are same as compared to CMOS levels equal to Vdd and this is the disadvantage of CPL. While switching CPL(Complementary Pass Transistor Logic) spikes are appeared on power supply and this is undesired. The Figure 5 shows CPL AND& NAND gate circuit.

METHODOLOGY

Vedic Multiplier is implemented by using HSPICE tool for 180nm Technology. In the design first the basic AND gate, OR gate and XOR gate are designed using conventional CMOS transistors and then using these gates Full adder is designed. The Full Adders are used to design 4 -bit Ripple carry adder. Partial products(PP) are generated using AND gates and Ripple carry adders(RCA) are used to add the partial products as per the Vedic multiplier architecture. In the similar way basic AND gate, OR gate and XOR gate are designed using CPL Logic and followed by Full adder and Ripple carry adder(RCA). Vedic Multiplier 2-bit is designed first and by using 2-bit Vedic Multiplier 4-bit Vedic Multiplier is designed using CMOS, CPL Logics. Vedic Multiplier 8-bit is designed using 4-bit Vedic Multipliers and Ripple Carry Adders as per the Architecture.

RESULTS

Vedic Multiplier is designed and simulated using HSPICE for 8-bit and 4-bit. The No of transistors , Power dissipation and Delay from simulation results are taken. Table 1 shows the conventional CMOS, CPL(Complementary Pass Transistor Logic) 4-bit Vedic Multiplier for 180nm Technology whereas Table 2 shows the conventional CMOS, CPL (Complementary Pass Transistor Logic) 8-bit Vedic Multiplier results for 180nm Technology.

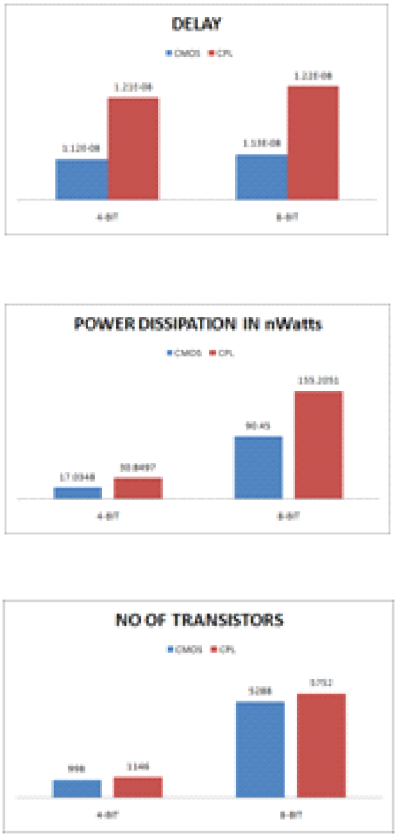

Figure 6 : Simulation Results

Table-1

S.NO	LOGIC	NO OF TRANSISTORS	POWER CONSUMPTION	DELAY
1	CMOS	998 0	17.0348nw	0.11188ns
2	CPL	1146 0	30.8497nw	0.12064ns

Table-2

S.NO.	LOGIC	NO OF TRANSISTORS	POWER CONSUMPTION	DELAY
1	CMOS	5288	90.4500nw	0.11256ns
2	CPL	5752	155.2051nw	0.12223ns

CONCLUSION

Fig. 6 shows simulation results for an Vedic Multiplier the CMOS Logic proves to be better than CPL transistors Logic. CMOS has shown less delay compared to CPL and hence CMOS is better. Similarly,

low power dissipation and less no of transistors were in CMOS than CPL. So CMOS logic is better than CPL for an Vedic Multiplier implementation. This work can be extended for implementing Vedic multiplier for DPL(Double Pass Transistor Logic).

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