VLSI Reliability in Europe

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ABSTRACT

A few points will be highlighted on the issue of VLSI reliability in Europe. First, there is a brief description of organizations involved in stimulating the activities on reliability by exchange of information (e.g., conferences) o r setting up research programs (e. g . , the well-known ESPRIT program). Within ESPRIT, a technical interest group on IC reliability for formulating particular needs and necessary improvements in education and research was formed. The first outcome was an annual European conference on reliability, the ESREF, the first of which was held in Bari in 1990. In addition to ESPRIT research projects, there are special (smaller) projects on reliability subjects. Two examples will be given and treated in more detail, namely, those on plastic-encapsulation and electro-static discharge.

Then some achievements in the area of firstly, oxide breakdown and secondly, plastic encapsulated IC's in temperature cycling are presented. Finally, a few opinions are given on new trends in reliability engineering, including reliability circuit simulation, if not already covered in the items mentioned above.

1. INTRODUCTION

In this paper my personal view on this topic of VLSI reliability in Europe is given. If you are expecting a full list of all activities and achievements of all the institutes and companies in Europe, then you will be disappointed. This paper is too short for such a goal; moreover, such an inventory would be very dull to read. Therefore, a few points will be highlighted. We start with cooperative reliability organizations in Europe followed by a few examples of reliability research programs and projects. Then I treat some examples of achievements in reliability research in which I was indirectly involved. They are in the area of process-related reliability (e.g., oxide breakdown) and package-related reliability (plastic encapsulated IC's in temperature cycling). Finally, a few opinions are given on new trends in reliability engineering, if they have not already been covered in the other items.

2. EUROPEAN ORGANIZATIONS

Organizations for standardization are the first to be mentioned in this section. Setting up and implementing standardization procedures for quality in general and reliability in particular can significantly contribute to the ultimate improvement of products. In Europe we have the organization CENELEC (abbreviation of the French name) and its Electronic Components Committee, CECC, which both play an important role in this area. In the CECC, makers and users of components are working together to formulate new procedures. In this way it is doing the same job that was traditionally done by the military organization in the United States (think of the Mil Handbooks and Milspec).

The Mil activities in the U.S. were strongly customer driven. This has given its procedures a strong mandate for the vendors of IC's. However, it is losing power these days for number of reasons. One is that

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it is difficult to stay in the forefront of new developments on quality control; it has to deal with a too small production compared to the nonmilitary markets. Larger production and larger series undoubtedly means better statistical control of processes with inherently better tools for higher quality and related reliability.

As a consequence, the nonmilitary users' requirements have taken over from Milspec. Perhaps this is not the complete picture but this is how it is perceived in Europe. An example of the nonmilitary programs is the Ford Q1, in the USA and also in Europe fully customer-driven and therefore successful in the implementation. We see in Europe that many chip vendors are first of all complying with their customer-driven programs instead of implementing CECC rules.

Among cooperative research organizations in Europe, ESPRIT is the major one. It is financing a large number of cooperative research projects, fitting its mission "programme for research and technological development in the field of information technology." For IC technology it is cooperating with Joint European Submicron Silicon (JESSI). In the next section I will give a couple of examples of ESPRIT projects in the area of VLSI reliability.

Within the ESPRIT, there is a Technical Interest Group (TIG) on IC reliability. It consists of representatives from the industry (both the vendors and the users) and the national laboratories, and it is chaired by Prof. Herman Maes of IMEC in Leuven. Its goal is to formulate particular needs and necessary improvements in the area of reliability. A few topics have been defined for further attention, namely:

i) failure analysis and fundamental failure mechanisms;
ii) IC package reliability;
iii) accelerated life testing and screening;
iv) reliability simulation;
v) IC reliability education.

The first outcome of the TIG activities is the setting up of an annual European conference on reliability. It is called the European Symposium on Reliability of Electron Devices Failure Physics and Analysis, a long name with an easy acronym: ESREF. The first one was held in Bari, Italy, in 1990, the second one in Bordeaux, France, in 1991 [l] . They were very succesful in attracting good papers and a large audience, and very likely it is the start of a good tradition like the IRPS and other conferences in the U.S.

Concerning the other activities and plans of the TIG, namely, when it comes to conducting the projects, i t is de-pending on the amount of money available within the total ESPRIT program. As to informal contacts and exchange of information, this is also being achieved within the frame-work of ESREF and also within other conferences such as INFOS (Insulating Films On Semiconductors). The latter, for example, had a workshop on hot carrier effects in 1992[2] .

It should be noted that all countries in Europe have their national learning societies with, in the larger countries, special branches dealing with reliability. A good example is the reliability chapter within the VDE, the German Institute of Electrical Engineers. This chapter has members from neighboring countries. In this way it has a European orientation even as a national organization.

3. EUROPEAN COOPERATIVE RELIABILIT YRESEARCH

In Europe there is a multitude of organizations and mentioning them all would be dull. In the previous section it is indicated that ESPRIT is the major one for supporting projects in the field of microelectronics. It is financed and managed by the Commission of the

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European Communities. One of the goals is to include reliability engineering as an essential part of the relevant projects, especially of the projects on technology development.

Also, separate (smaller) projects are supported with emphasis on reliability. This is feasible when particular re-search has to be done for the reliability of many products in different technologies. Two examples will be given here: firstly, the PLASIC project (Performance and reliability of PLastic encapsulated CMOS ASIC's) and secondly, the EPST project (ESD Protection for Submicron Technologies).

For the PLASIC project the consortium consists of Mi-etec Alcatel (vendor) in Belgium. SGS-Thomson Micro-electronics (vendor) in France, SEL Alcatel (user) in Ger-many, Elektronik Centralen (institute) in Denmark, and NMRC (institute) in Ireland.

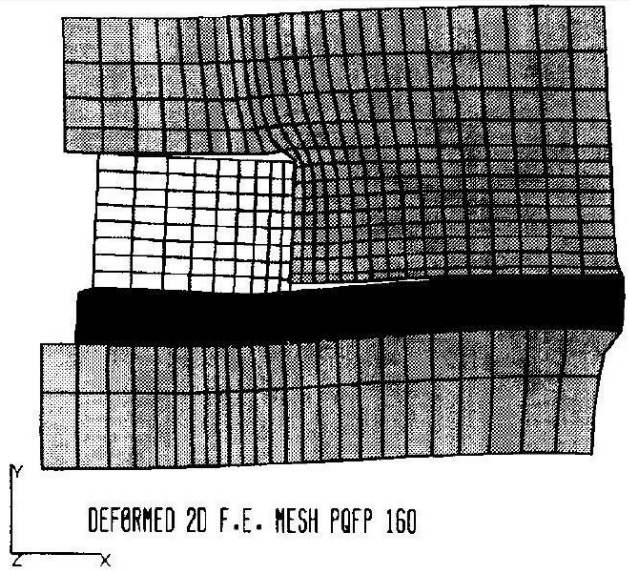

Fig. 1. Result of the calculation of deformation of PQFP 160 in the presence of delamination. View of an deformed finite element mesh in the region close to the die edge. (G . Kelly et al.) [2].

The activities form a broad spectrum comprising materials and process studies electro-thermal characterization of plastic packages, reliability evaluation (temperature cycling and moisture tests), thermo-mechanical modeling, etc. **A** few more words will be devoted here to the last activity because it illustrates the approach followed to gain understanding of the cause of low reliability.

Traditionally, thermo-mechanical modeling is carried out under the assumption of elastic deformation in homogeneous media, which means no cracks in the plastic and no delamination between plastic and silicon die. However, in temperature cycling there is a large risk of delamination because of the large mechanical stresses. This delamination starts at the comers and edges of the die [3] ,while delamination can also occur at the interface between leadframe and plastic. The result is an exceptionally large force on ballbonds with a large probability for loose bond wires (see also Section V of this paper). Within the project, NMRC started with taking delamination into account in the calculation of the mechanical stresses and strain. This was done on a 160-pin plastic quad flat pack (PQFP160). For the material properties, please refer to the original publication [4]. Fig. I shows a result with the deformed finite element mesh of the PQFP160 in the region close to the die edge i n the presence of delamination. This illustrates the large deformations occurring after delami-nation.

This project is an example of how cooperative research projects are executed i n Europe. Industrial laboratories work together with governmental institutes from different countries in Europe. The institutes contribute mainly in the development of analytical methods and modeling, the companies on technology development and the application of the results.

It should be noted that Europe is at a disadvantage in the field of plastic encapsulation because nearly all assembly is in the Far East or at least outside Europe. Moreover, the major molding compound vendors are outside Europe. This is far from a good situation for a close cooperation between compound vendors, assembly lines, and IC manufacturers. This PLASIC project nevertheless is aiming at accomplishing such a goal within these disadvantageous boundary conditions.

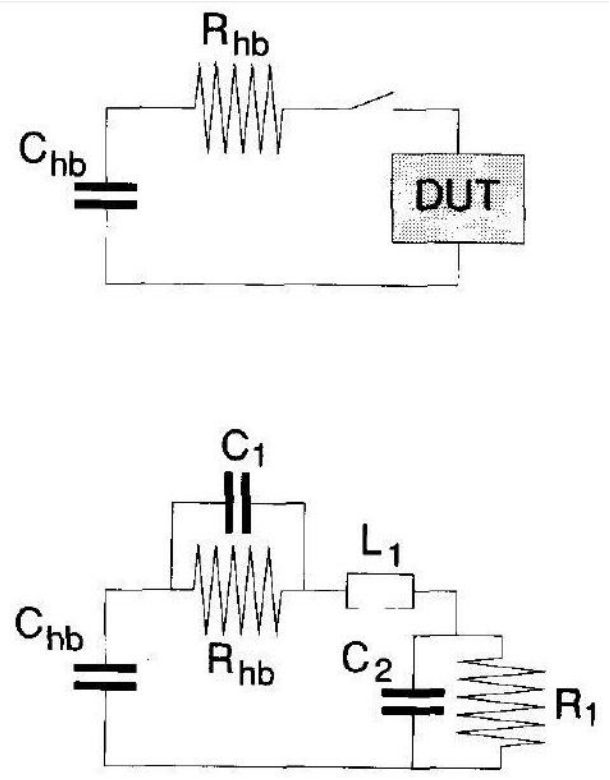

Fig. 2. The equivalent circuit for the human body model electro-static discharge; top: according to MIL STD 883U3015.7, bottom: including the main parasitic elements.

The second example of an ESPRIT project with a large reliability emphasis is the EPST project on Electro Static Discharge (ESD) protections. The consortium consists of Siemens, Philips, IMEC, and the Technical University of Munich. The activities consist of a comparison of different ESD testers, development of a new test setup, development of improved protection circuits, all supported by modeling of test setups as well as protection circuits.

The first outcome of this project was the large spread in the results obtained with 11 different testers although all had the same setup, namely, the human body model (HBM). This setup is very simple; it simulates the handling of devices by charged human beings. It has been standardized by the Mil Standard in the USA: MIL STD 883C/3015.7. The equivalent circuit is given in Fig. ***2*** (top). The capacitor C_{hb} in Fig. 2 is discharged in the test. This results in a voltage or current pulse through the DUT. The standard specifies that R_{hb} = 1500&!±1%, C_{hb} = 100 pF±10%. However, in practice several parasitic are present, for instance, a stray capacitance of the test board at the device under test (DUT in Fig. ***2)*** **.** This capacitance is not detected when calibration is carried out according to MIL STD because then the DUT is short-circuited. It would be much better to have a load resistance R_l of, say, 1000 &! in the calibration setup. These and other findings and considerations lead to the complete equivalent circuit given at the bottom of Fig. ***2*** [5].

The insufficient specification of the parasitic elements (capacitances C_1 and C_2 and inductance L_1), and the resulting differences among testers, are very likely the cause of the large spread in tester results. This comparison of testers within the project goes back to an earlier investigation at Philips (5). For other ESD studies at Philips, excellent work of Ajith Amerasekera and coworkers is referred [6], [7].

The researchers at IMEC were able to derive an analytical expression for the (current-time) behavior of the ESD testers including their parasitic elements [8]. From simulation and curve fitting to the experimentally determined pulses the value of these elements could be derived. Of course, the next step to be expected is a tester optimization with respect to these parasitic elements and subsequent

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standardization of the test. When one considers that there are other test setups or configurations, such as Machine Model and Charged Device Model (yet to be thoroughly investigated) it is clear that there is a long way to go. The project consortium has decided to accomplish standardization but to achieve this in close collaboration with the EOSESD Association in the U.S. These two projects illustrate how cooperative research projects are executed and how different companies/institutes work together. In some areas it takes often not only a European but also a global approach.

4. PROCESS-RELATED RELIABILITY

Process-related reliability is that part of reliability engineering that is dealing with materials and basic structures in the integrated circuits. Tests are carried out on test structures and quite often on-the-wafer with relatively high acceleration factors. Examples are oxide breakdown tested on capacitors, electro-migration tested on metal stripes, and hot carrier effects on single transistors. [9,10] He adopted and worked out the concept of charge-to-breakdown brought forward by Harari. This has led to a large number of contributions in this field from him and his coworkers on the constancy of the charge-to-breakdown Q_{BD} as a function of stress current, the relation between voltage stress and current stress, the statistics of breakdown, the defect-related part in a statistical distribution of failing capacitors, the trapping of charge in the pre-breakdown phase, and last but not least, the mechanism of oxide breakdown. This work has been treated in a number of review papers [11,12].

It is clear now that one can make a distinction between the defect-related part and the intrinsic part in a breakdown distribution. The defects form a reliability hazard: they can give an early failure in time-dependent dielectric breakdown which means a short life. For a calculation of the actual lifetime of a product, or rather the mean and spread in life time of a large number of products, one needs the value of the acceleration factors for derating stress results to practical use conditions. In the traditional concept, breakdown of a dielectric was thought to be caused by a high field. In that case one needs the field acceleration for derating high-field stress results. In the concept of Q_{BD} one needs to know the current level in the oxide at practical use conditions (apart from the assumption of the independence of Q_{BD} from oxide current). However, one only knows the voltage or oxide field during operation. Therefore, derating in this case means an assumption about the current-field relation for the oxide.

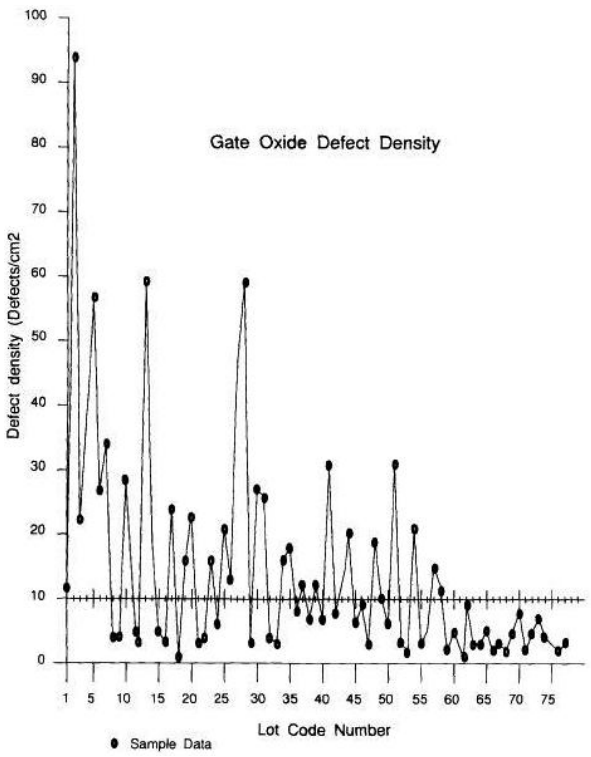

Fig. 3. Gate oxide defect density in consecutive lots of wafers. Courtesy: M. Pinto, Philips Semiconductor, Nijmegen.

Professor Chenming Hu and coworkers at Berkeley have done a good job on this derating for the estimation of oxide reliability (see [13] and its references). They were able to give a consistent description of the experiments of their own as well as

of others in terms of a limited number of parameters. However, the physical mechanism underlying their model is in my opinion debatable. It is in terms of hole generation in the oxide followed by trapping (and some recombination). The result is a buildup of positive charge leading to current increase and breakdown it seems that the same set of parameters but a different physical mechanism would do the job as well.

Dr. Wolters observed, as is already mentioned above, the constancy (of the average value) of Q_{BD} as a function of oxide current. According to him this precludes the avalanche multiplication as a stepping stone in the oxide breakdown mechanism because the multiplication is strongly field dependent. The constancy of Q_{BD} has been nicely corroborated by researchers in Japan [14]. Moreover, the electron transport studies at IBM, Yorktown Heights (see, for instance, [15] demonstrate that avalanche multiplication is an unlikely process.

Wolters' physical mechanism for oxide breakdown is the following. At the anode, electrons from a Fowler-Nordheim tunnel current loose their energy to the SiO_2 lattice where it is used to break some bonds. This bond breaking proceeds from anode to cathode forming a conductive path. Upon discharge of the capacitor through this path the material is blown and the capacitor broken down. This mechanism is able to explain virtually all related phenomena. However, it should be stated here that there is not a general consensus about the mechanism. Some more experimental work is still needed to give a sound base to all modeling.

The concept of Q_{BD} and the related defect density

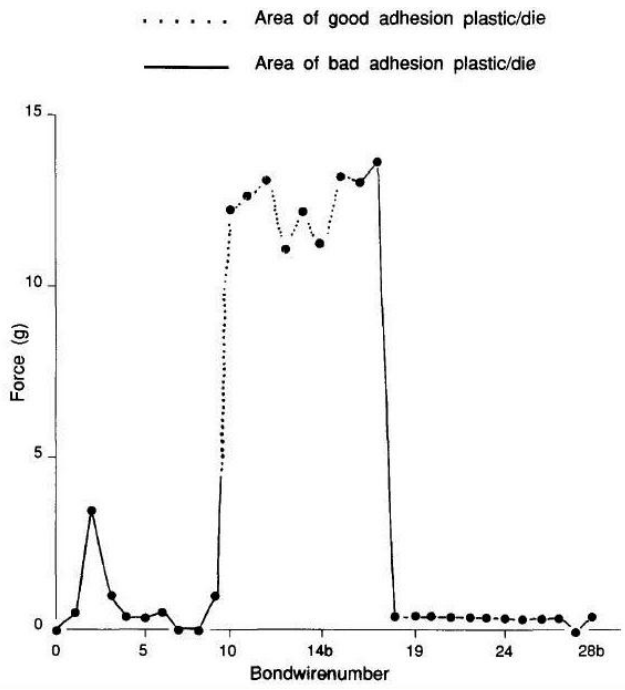

Fig. 4. Pulling force of bond wires in a product after SO0 cycles in a temperature cycling test. Indicated are the regions of good adhesion (dashed line) and bad adhesion plastic die (solid line).
Courtesy : A. van der Wijk, Philips Semiconductor, Stadskanaal.

has found a new application in Statistical Reliability Monitoring (SRM). In the SRM approach particular process parameters are measured that are relevant for reliability and that are compatible with the concepts of Statistical Process Control (SPC). It appears that Q_{BD} measurements and the derived defect density can do the job for oxide-related reliability. It is a relatively short test of a few minutes on simple capacitor structures on the wafer with a fast feedback to process engineering. Although the measured defect density is not directly yielding a product lifetime, it can be the input for a program of continuous process improvement with inherent product improvement.

An example of a series of measurements is given in Fig. **3.** It can be seen that the oxide defect density is steadily de-creasing which was actually the result of corrective actions based on the presented sample data. The corrective actions were predominantly on improving cleaning procedures.

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I have given this example of oxide breakdown work also to demonstrate that in this field of oxide breakdown there is not a difference in approach between the U.S., Japan, and Europe.

5. PACKAGE-RELATED RELIABILITY

The subject of package-related reliability deals with the reliability of integrated circuits encapsulated in plastic. We have to face large mechanical stresses on the chip with inherent reliability hazards. A few years ago I wanted to discuss this subject but the reaction I got was "how silly it would be to put these nice and expensive microprocessors in dirty plastic." Since then times have changed and many nice and expensive chips are going into plastic packages.

I recognized that there was a large risk for Philips of lagging behind in the development of high reliability plastic-encapsulated IC's. The reasons are discussed in Section III of this paper. From companies in Japan it is learned that they were using the Scanning Accoustical Tomograph (SCAT) for investigating particular reliability mechanisms. We at Philips bought the same piece of equipment, the first one outside Japan. It should be noted that this type of equipment had already been in use in Japan for many years. With the SCAT technique we discovered [3] that delamination at the die-plastic interface is a major reliability hazard: it gives the well-known pattern shift of the (top) metallization on the die. Moreover, resulting large forces on ball bonds could give degradation. The result of an investigation in this direction is given in Fig. 4. It is actually a wire pull test on an IC that has been subjected to 500 cycles in a temperature cycling test. The amount of delamination or bad adhesion was determined by the SCAT technique before decapsulation and wire pull test. The solid line is the area of bad adhesion. We can clearly see that the bond wires with low pull strength are in the area of bad adhesion. This is consistent with a model in which delamination between plastic and die gives extra mechanical forces on the bond balls [16, 17].

A major concern in Europe is the environment. How this can affect, reliability engineering is shown in the following example. In temperature cycling we have basically two types of tests. In both tests the samples are interchanged between two chambers at different temperatures but in one test the chambers contain air and in the other they contain liquids. The abbreviations for the tests used here are TMCL (temperature cycling) and TMSK (thermal shock), respectively. For the usual large temperature swing of -65°C to l50°C the liquids are chloro-fluoro-carbon compounds which are now known to be detrimental to the environment.

Therefore, we carried out an investigation into the dif-ferences between the two types of tests with the aid of the SCAT technique. The result is given in Fig. 5, which shows the percentage of delamination as a function of the number of cycles. It can be concluded that the evolution of the delamination is similar in both tests. Hopefully, these results contribute to completely phasing out the shock tests which use hazardous compounds.

6. NEW TRENDSIN RELIABILITY ENGINEERING

New trends in reliability engineering are strongly related to new trends in technology. These are smaller feature sizes on the chip at one hand, and larger chips at the other hand. The smaller feature sizes go together with thinner (gate) oxide layers and narrower spacings between metal patterns. This implies a higher reliability risk especially in the so-called early-failure-rate regime which is so strongly related to workmanship and defect density. This brings forward the big issue of continuous quality and reliability improvement. This will be done with the aid of better failure analysis techniques and with concepts like Statistical Reliability Monitoring. The larger chips bring greater reliability hazards due

to mechanical stresses as discussed in Sections III and V. Also, here we have the same issue of continuous quality improvement via better analysis. modeling, and process control.

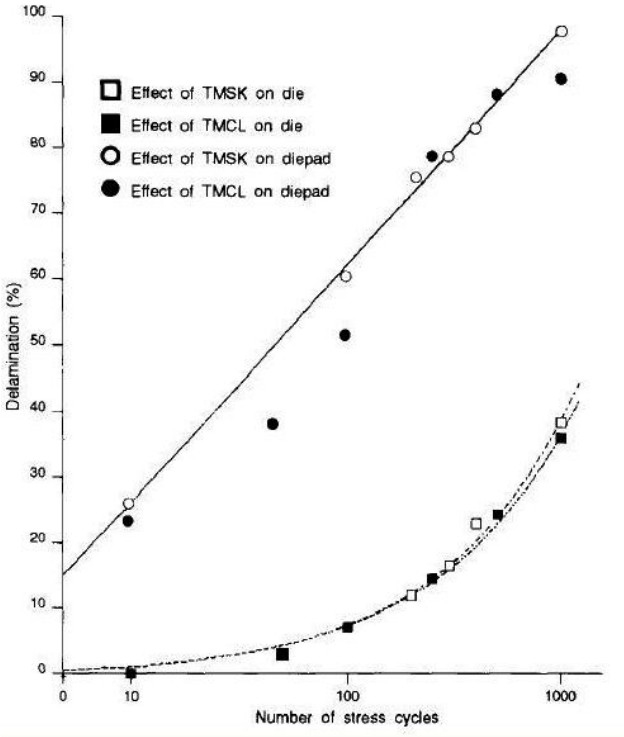

Fig. 5. Percentage of delamination on die and diepad of a plastic encapsulated IC in temperature cycling tests in either liq-uid-to-liquid (Thermal Shock) or air-to-air (Temperature Cycling). Courtesy of A. van der Wijk, Philips Semiconductor, Stadskanaal. 0 Effect of Thermal Shock on die H Effect of Temperature Cycling on die 0 Effect of Thermal Shock on diepad Effect of Temperature Cycling on diepad

A new trend, not mentioned above or in the previous sections but relevant for proper design, is the development and application of reliability circuit simulators. We found that the hot carrier related lifetime of CMOS products differed considerably from that derived from experiments on transistors [17]. This has to do with the relatively low sensitivity of these particular products to the hot carrier effects and by duty cycle effects. The relation between transistor life and product life could be verified by circuit simulation, i.e., a computer calculation of the electrical performance of (part of) the circuit taking into account the reliability parameters.

At the moment this tool is being further developed in Europe as well as elsewhere [19]. The designers are leaving the era of bread boarding for reliability entering full simulation, which actually means that their reliability-related design rules come from tests on test structures only. They are now entering full simulation.

7. CONCLUSIONS

VLSI reliability in Europe means a multitude of organizations, projects, and activities. Only a few examples could be given in this paper. From this one may derive that reliability engineering practice as such does not differ significantly from that in other regions, especially not from that in the U.S.

Research projects are executed in cooperation between industries and research institutes of different countries in Europe. However, exchange of information on experimental results, models, standards etc., is taking place on a global scale, in this way forwarding the total field of VLSI reliability.

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