Modeling of Sub Threshold Current and Sub Threshold Swing of Short-Channel Fully-Depleted SOI MOSFET with Back-Gate Control

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Abstract

The present paper deals with the analytical modeling of subthreshold characteristics of short-channel fully-depleted recessed-source/drain SOI MOSFET with back-gate control. The variations in the subthreshold current and subthreshold swing have been analyzed against the back-gate bias voltage, buried-oxide (BOX) thickness and recessed source/drain thickness to assess the severity of short-channel effects in the device. The model results are validated by simulation data obtained from two-dimensional device simulator ATLAS from Silvaco.

1. INTRODUCTION

It has been known that the short-channel effects are well suppressed in a FD SOI MOSFET, when the silicon channel thickness (t_{Si}) is less than or equal to one-fourth of the channel length (L). However, in sub 30 nm channel length regime, t_{Si} needs to be scaled below 5nm; therefore, the large parasitic series resistance and threshold voltage sensitivity to t_{Si} variation become serious issues [1, 2]. The extended source and drain offer low source and drain resistance, respectively, and facilitate better source and drain contacts and consequently decrease the total series resistance [3]. The presence of a back-gate in FD Re-S/D SOI MOSFETs could be a potential option to improve the device performance in terms of less parasitic series resistance, on-current (I_{on}) improvement, and off-current (I_{off}) suppression as well [4]. Keeping in view the above facts, an attempt has been made in this paper to present a theoretical and simulation-based study of subthreshold swing and subthreshold current of the FD Re-S/D SOI MOSFETs with back-gate control.

2. DEVICE STRUCTURE

The schematic structure of a Re-S/D UTB SOI MOSFET with back-gate control is shown in Fig.1, where, L is the gate length, t_{Si} is the Si film thickness, t_{ox} is the gate oxide thickness and t_{box} is the buried oxide thickness. N_a, N_d and N_{sub} represent channel, source/drain, and substrate doping concentrations respectively. V_{Gs}, V_{DS} and V_{BG} are the gate to source, drain to source, and back-gate voltages, respectively. The symbols of work functions of front- and back-gate materials are taken to be ϕ_{FM} and ϕ_{BM} respectively.

In the present structure, since we have considered a separate back gate on the substrate as done in Ref. [5], the substrate doping really does

not matter much and the substrate only provide mechanical support to the structure. The doping density in the channel region is considered to be uniform and the influence of charge carriers and fixed oxide charge on the electrostatics of the channel is neglected. The x- and y-axes of the 2D structure are considered to be along the channel-gate oxide interface and the source-channel interface respectively, as shown in Fig.1.

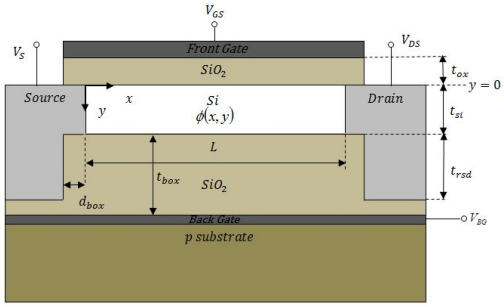

Fig.1: The Schematic Structure of the Re-S/D FD SOI MOSFET with Back-Gate control

The other parameters used in modeling and simulation are detailed in Table 1.

Table-1: Device Dimensions and Parameters used for Modeling and Simulation

Parameters	Symbol	Values
Front-gate work-function	ϕ_{FM}	4.71 eV, 4.8 eV
Back-gate work-function	ϕ_{BM}	4.71 eV, 4.8 eV
Channel Doping	N_a	10^{15} cm^{-3}
Source/Drain Doping	N_d	10^{20} cm^{-3}
Substrate Doping	N_{sub}	10^{15}
Silicon Thickness	t_{Si}	6-10 nm
Gate Oxide Thickness	t_{ox}	1.5-3 nm
Buried Oxide Thickness	t_{box}	40-80 nm
The depth of S/D in the buried oxide	t_{rsd}	0- 25 nm
Recessed Length	d_{box}	3 nm
Channel Length	L	20-120 nm
Gate-to-Source Voltage	V_{GS}	-0.2 V to 0.6 V
Drain Voltage	V_{DS}	0.05 V
Back-gate Voltage	V_{BG}	-5 to 2 V

3. THEORETICAL MODELING

The two-dimensional channel potential $\phi(x,y)$ can be obtained by solving the following 2D Poisson's equation

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{Si}};$$

$$0\le x\le L,\ 0\le y\le t_{Si} \qquad (1)$$

The potential profile in the vertical direction (y-dependence of $\phi(x,y)$) in the channel can be approximated by following parabolic function [6].

$$\phi(x,y)=\phi_f(x)+C_1(x)y+C_2(x)y^2 \quad (2)$$

where, $\phi_f(x)=\phi(x,0)$ is the surface potential at SiO_2/Si interface and the arbitrary coefficients $C_1(x)$ and $C_2(x)$ are the functions of x only. These coefficients are to be determined using the boundary conditions and can be written as

$$C_1(x)=\frac{C_{ox}}{t_{Si}C_{Si}}\left[\phi_{s1}-\left(V_{GS}-V_{FB1}\right)\right] \qquad (3)$$

$$C_2(x)=\frac{C_{rsd}}{2t_{Si}^{\ 2}.C_{Si}}\left[V'_{DS}\right]+\frac{C_{box}}{2t_{Si}^{\ 2}.C_{Si}}\left[V'_{BG}\right]+\frac{C_{ox}}{2t_{Si}^{\ 2}.C_{Si}}\left[V'_{GS}\right] \qquad (4)$$

Now, the expression for $\phi(x,y)$ is obtained by substituting the values of $C_1(x)$ and $C_2(x)$ into Eq. (2). Thus, the potential can be written as

$$\phi(x,y)=\phi_f(x)+\frac{C_{ox}}{t_{Si}.C_{Si}}\left[\phi_f(x)-V'_{GS}\right] y+\left\{\frac{C_{rsd}}{2t_{Si}^{\ 2}.C_{Si}}\left[V'_{DS}-2\phi_b(x)\right]+\frac{C_{box}}{2t_{Si}^{\ 2}.C_{Si}}\left[V'_{BG}-\phi_b(x)\right]+\frac{C_{ox}}{2t_{Si}^{\ 2}.C_{Si}}\left[\phi_f(x)-V'_{GS}\right]\right\}y^2 \qquad (5)$$

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Further, the following differential equation of front-surface potential, ϕ_f has been obtained using $\phi(x,y)$ of Eq. (2) into Eq. (1) at $y=0$

$$\frac{d^2\phi_f(x)}{dx^2}-\alpha_f\phi_f(x)=\beta_f \tag{6}$$

where, α_f and β_f are

$$\alpha_f=2\frac{1+\left(\frac{C_{ox}\left(C_{Si}+2C_{rsd}+C_{box}\right)}{C_{Si}\left(2C_{rsd}+C_{box}\right)}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{2C_{rsd}+C_{box}}\right)} \tag{7}$$

$$\beta_f=\frac{qN_a}{\varepsilon_{Si}}-V'_{GS}A_{1f}-V'_{DS}A_{2f}-V'_{BG}A_{3f} \tag{8}$$

$$A_{1f}=\frac{\left(\frac{2C_{ox}\left(C_{Si}+2C_{rsd}+C_{box}\right)}{C_{Si}\left(2C_{rsd}+C_{box}\right)}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{2C_{rsd}+C_{box}}\right)}$$

$$A_{2f}=\frac{\left(\frac{2C_{rsd}}{2C_{rsd}+C_{box}}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{2C_{rsd}+C_{box}}\right)}$$

$$A_{3f}=\frac{\left(\frac{2C_{box}}{2C_{rsd}+C_{box}}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{2C_{rsd}+C_{box}}\right)} \tag{9}$$

Eq. (6) can be solved as

$$\phi_f=A_f.e^{\sqrt{\alpha_f}x}+B_f.e^{\sqrt{\alpha_f}x}-\frac{\beta_f}{\alpha_f} \tag{10}$$

Now, the coefficients (A_f , B_f) of Eq. (10) are determined using the boundary conditions as

$$A_f=\frac{\beta_f\left(e^{\sqrt{\alpha_f}L}-1\right)+\alpha_f\left[V_{bi}\left(e^{\sqrt{\alpha_f}L}-1\right)+V_{DS}e^{\sqrt{\alpha_f}L}\right]}{\alpha_f\left(e^{2\sqrt{\alpha_f}L}-1\right)} \tag{11}$$

$$B_f=\frac{e^{\sqrt{\alpha_f}L}\left\{\beta_f\left(e^{\sqrt{\alpha_f}L}-1\right)-\alpha_f\left[V_{bi}\left(1-e^{\sqrt{\alpha_f}L}\right)+V_{DS}\right]\right\}}{\alpha_f\left(e^{2\sqrt{\alpha_f}L}-1\right)} \tag{12}$$

Similarly, the following differential equation of back-surface potential, ϕ_b has been obtained using $\phi(x,y)$ of Eq. (5) into Eq. (1) at $y=t_{Si}$

$$\frac{d^2\phi_b(x)}{dx^2}-\alpha_b\phi_b(x)=\beta_{,b} \tag{13}$$

where, α_b and β_b are

$$\alpha_b=2\frac{1+\left(\frac{\left(C_{ox}+C_{Si}\right)\left(2C_{rsd}+C_{box}\right)}{C_{ox}C_{Si}}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{C_{ox}}\right)} \tag{14}$$

$$\beta_b=\frac{qN_a}{\varepsilon_{Si}}-V'_{GS}A_{1b}-V'_{DS}A_{2b}-V'_{BG}A_{3b} \tag{15}$$

Here

$$A_{1b}=\frac{2}{t_{Si}^2\left(1+2\frac{C_{Si}}{C_{ox}}\right)}$$

$$A_{2b}=2\frac{\left(\frac{C_{rsd}}{C_{ox}}+\frac{C_{rsd}}{C_{Si}}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{C_{ox}}\right)}$$

$$A_{3b}=2\frac{\left(\frac{C_{box}}{C_{ox}}+\frac{C_{box}}{C_{Si}}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{C_{ox}}\right)} \tag{16}$$

Using the boundary conditions in solving Eq. (5), gives the following equation for the back-surface potential

$$\phi_b=A_b.e^{\sqrt{\alpha_b}x}+B_b.e^{\sqrt{\alpha_b}x}-\frac{\beta_b}{\alpha_b} \tag{17}$$

Similarly, the coefficients A_b , B_b are determined as

$$A_b = \frac{\beta_b\left(e^{\sqrt{\alpha_b}L}-1\right)+\alpha_b\left[V_{bi}\left(e^{\sqrt{\alpha_b}L}-1\right)+V_{DS}e^{\sqrt{\alpha_b}L}\right]}{\alpha_b\left(e^{2\sqrt{\alpha_b}L}-1\right)} \quad (18)$$

$$B_b = \frac{e^{\sqrt{\alpha_b}L}\left\{\beta_b\left(e^{\sqrt{\alpha_b}L}-1\right)-\alpha_b\left[V_{bi}\left(1-e^{\sqrt{\alpha_b}L}\right)+V_{DS}\right]\right\}}{\alpha_b\left(e^{2\sqrt{\alpha_b}L}-1\right)} \quad (19)$$

The minimum of the front- and back- surface potential $\phi_{f\min,b\min}$ would determine the threshold voltage of the device. The obtained expression is

$$\phi_{f\min,b\min} = 2\sqrt{A_{f,b}B_{f,b}} - \frac{\beta_{f,b}}{\alpha_{f,b}} \quad (20)$$

3.1 Subthreshold Current Formulation

The subthreshold current is mainly dominated by the diffusion phenomenon and is proportional to the carrier concentration at the minimum surface potential position (virtual cathode) as calculated as

$$V_{th} = \begin{cases} V_{thf}, & \text{for} \quad \phi_{f,\min} > \phi_{b,\min} \\ V_{thb}, & \text{for} \quad \phi_{f,\min} < \phi_{b,\min} \end{cases}$$

Therefore, by employing the 2D surface potential function and following the methodology used in Ref. [7], the expression of subthreshold current can be written as follows:

$$I_{sub} = K\int_0^{t_{Si}} \exp\left(\frac{\varphi_{vc}(y)}{V_T}\right)dy \quad (21)$$

where, $\varphi_{vc}(y)$ is the virtual cathode potential.

Now, after solving the Eq.(21), the obtained final subthreshold current expression, I_{sub} is

$$I_{sub} = KV_T\left[\frac{I_f}{E_f} + \frac{I_b}{E_b}\right] \quad (22)$$

where,

$$I_f = \exp\left(\frac{\phi_{vc}(y=0)}{V_T}\right) - \exp\left(\frac{\phi_{vc}(y=y_m)}{V_T}\right) \quad (23)$$

$$I_b = \exp\left(\frac{\phi_{vc}(y=y_m)}{V_T}\right) - \exp\left(\frac{\phi_{vc}(y=t_{Si})}{V_T}\right) \quad (24)$$

$$E_f = (\phi_{vc}(y=0) - \phi_{vc}(y=y_m))/y_m \quad (25)$$

$$E_b = (\phi_{vc}(y=y_m) - \phi_{vc}(y=t_{Si}))/(t_{Si}-y_m) \quad (26)$$

3.2 Subthreshold Swing Formulation

This section presents the modeling of subthreshold swing of short-channel Re-S/D SOI MOSFETs with Back-Gate Control. Sub Threshold Wwing (S) of Re-S/D SOI MOSFETs with Back-Gate Control can be written as [7]

$$S = \begin{cases} \ln 10.V_T\left(1+\dfrac{C_{Si}(2C_{rsd}+C_{box})}{C_{ox}(C_{Si}+2C_{rsd}+C_{box})}\right) \\ \left(\dfrac{1+e^{\sqrt{\alpha_s}L}}{1+e^{\sqrt{\alpha_s}L}-e^{\sqrt{\alpha_s}\phi_{f\min}}-e^{\sqrt{\alpha_s}(L-\phi_{f\min})}}\right) \text{ for } \phi_{f\min} > \phi_{b\min} \\ \ln 10.V_T\left(1+\dfrac{(C_{ox}+C_{Si})(2C_{rsd}+C_{box})}{C_{ox}C_{Si}}\right) \\ \left(\dfrac{1+e^{\sqrt{\alpha_s}L}}{1+e^{\sqrt{\alpha_b}L}-e^{\sqrt{\alpha_b}\phi_{f\min}}-e^{\sqrt{\alpha_b}(L-\phi_{b\min})}}\right) \text{ for } \phi_{b\min} > \phi_{f\min} \end{cases} \quad (27)$$

4. RESULTS AND DISCUSSION

In this section, we have compared the analytical results obtained from the proposed models with the numerical simulation data obtained by simulating the device structure under consideration with a commercially available 2D device simulator ATLAS™ [8].

4.1 Sub Threshold Current

The sub threshold current (I_{Sub}) with the gate voltage for three different buried oxide thicknesses (t_{box}) is plotted in Fig.2. It should be noted that the present subthreshold current model is based on only the diffusion phenomenon of current transport, and therefore, the sub threshold current can be observed in agreement with the simulation results below the threshold voltage of the device. It is observed from Fig. 2 that for the fixed values of V_{GS} the sub threshold current is decreased with the decrease in BOX thickness. This decrease of I_{Sub} using a thinner BOX may be due to larger impact of back-gate reverse bias on it. The sub

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threshold current (I_{Sub}) variation with the gate to source voltage V_{GS} for different recessed-source/ drain thickness (t_{rsd}) is considered in Fig. 3. It is found that at t_{rsd} = 0nm (conventional SOI with back-gate), I_{Sub} is ~ $2*10^{-10}$ A/μm and as increases to 25nm, becomes ~ $5*10^{-10}$ A/μm. It is due to the fact that a deeper recessed source/drain offers higher short-channel effects due to the stronger coupling between recessed-source/drain and channel region. Figure 4 displays the impact of different back-gate voltages over the sub threshold current variation. The sub threshold current is found to be decreased with decreasing back-gate voltage. This is because the reverse back-gate voltage decreases the front surface barrier height which, in turn, causes the inversion layer at the front-surface of the channel like conventional SOI MOSFETs.

4.2 Sub Threshold Swing(S)

Figure 5 shows the variation of sub threshold swing (*S*) against the device channel lengths for different BOX thicknesses. The parameter *S* is found to be increased with the shrinkage of channel length < 70nm resulting in the poor switching characteristics of the device. However, for a fixed gate-length, the switching characteristics are observed to be improved with decreasing values of gate oxide thickness. Since, the gate will be in better position to control the channel for smaller gate oxide thickness, the above results seem to be well justified. The impact of back-gate voltage on the subthreshold swing (S) is presented in Fig. 6. It is observed that the reverse back-gate bias voltage can improve switching characteristics immensely. As the reverse back-gate voltage decreases from -1V to -3V the switching characteristics are found to be improved by ~ 30mV/Dec by keeping the other parameters constant.

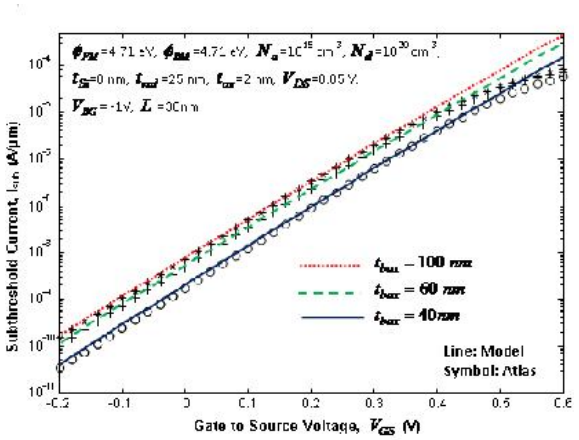

Fig.2: Sub Threshold current versus gate to source voltage for different buried oxide (BOX) thicknesses.

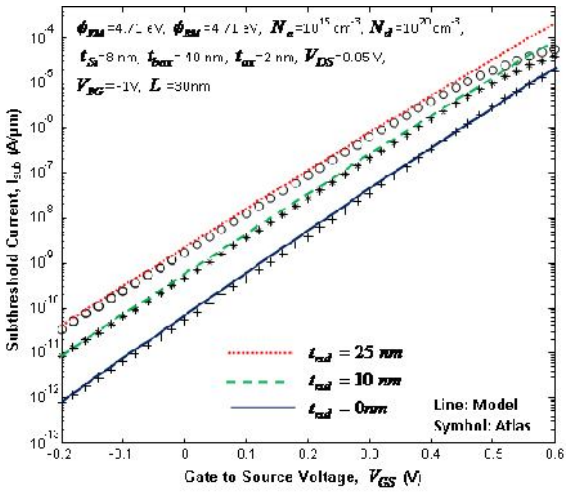

Fig.3: Sub Threshold current versus gate to source voltage for different recessed source/drain thicknesses

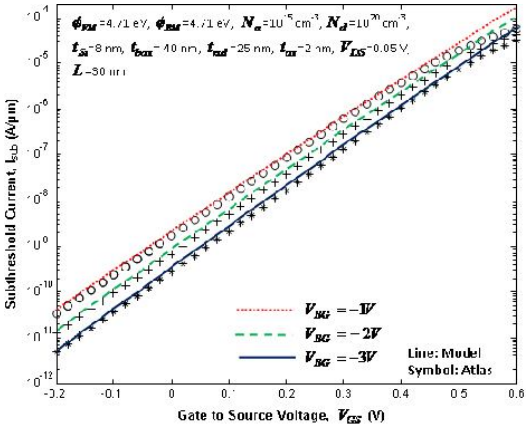

Fig.3: Sub Threshold current versus gate to source voltage for different back-gate voltage

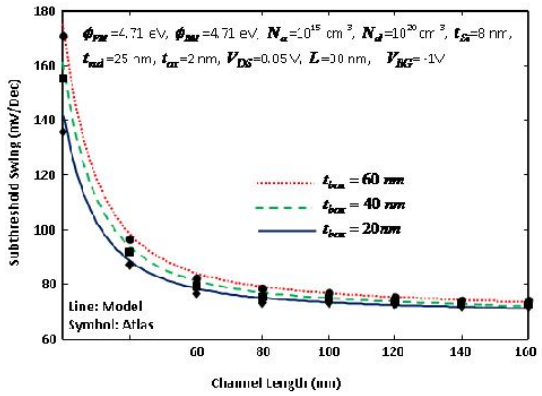

Fig.5: Subthreshold swing variation with channel length for different buried oxide (BOX) thicknesses

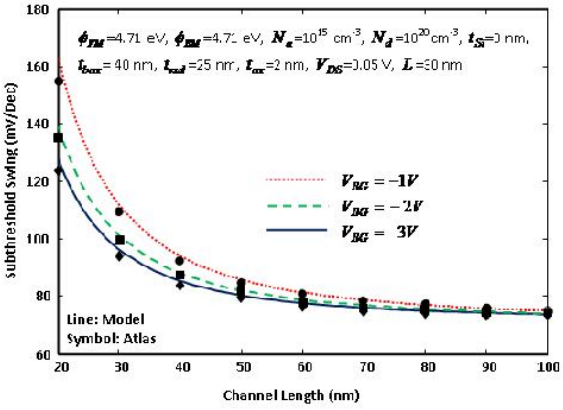

Fig.6: Subthreshold swing versus channel length for different back-gate voltages

5. CONCLUSION

In this paper, sub threshold swing and sub threshold current models are formulated for short-channel back-gated Re-S/D SOI MOSFETs. The variations in the sub threshold current and subthreshold swing have been analyzed against the back-gate bias voltage, buried-oxide (BOX) thickness and recessed source/drain thickness. It has been found that a negative back-gate bias voltage shift the peak of inversion charge density from back-channel to the front-channel resulting in an excellent short-channel-effects immunity in the device. The sub threshold swing roll-up of the Re-S/D SOI MOSFET are found to be significantly decreased with reverse back-gate bias voltage compared to the positive or no potential at the back-gate. Hence, the use of negative bias voltage may be a potential solution to reduce the short-channel effects in the Re-S/D SOI MOSFET. The excess short-channel effects owing to the recessed-source/drain thickness may be compensated by carefully applying the reverse back-gate bias voltage. Moreover, the model results are found to be in very good agreement with numerical simulation data obtained from ATLAS™.

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