

SPICE Simulation of Memristor Series and Parallel

Mohd Ahmer^{*1}, Abdul Sajid² & M. Yusuf Yasin³

1,2&3 Research Scholar, ECE Department, Integral University, Lucknow, (U.P.) India.
e-mail : mhdahmer@gmail.com^{*1}, msajid@iul.ac.in², mmyasin@rediffmail.com³

Publication Info

Article history :

Received : 14th Nov. 2017

Accepted : 01st Dec. 2017

DOI : 10.18090/samriddhi.v9i02.10867

Keywords :

Memristor, HSPICE

*Corresponding author :

Mohd Ahmer

e-mail : mhdahmer@gmail.com

Abstract

Memory Resistors also known as Memristors, is a nonlinear resistor with memory. It is the fourth basic circuit element except resistor, capacitor and an inductor. The capability of memorizing its resistance makes its useful for designing of non volatile memory and in neural networks. This paper aims at study of Memristors characteristics. We first analyze and model the characteristics of Memristor with HSPICE and then study its behavior for series and parallel combination.

1. INTRODUCTION

A Memristor is a two terminal device whose resistance depends on one or more internal state variables of the device. It was first mathematically introduced by theorist Leon Chua [1]. Memristor is defined by a state-dependent Ohm's law. Its resistance depends on the entire past signal waveform of the applied voltage, or current, across the memristor. Through memristor, one can achieve functionalities that are not possible through existing circuit elements. Its unique applications are in ultra dense information storage, neural networks, spintronics and programmable devices.

It is a two terminal device that relates the two mathematical variables q and φ as follows:

$$q(t) \triangleq \int_{-\infty}^t i(\tau) d\tau \quad (1)$$

$$\varphi(t) \triangleq \int_{-\infty}^t v(\tau) d\tau \quad (2)$$

Here, charge ' q ' and flux ' φ ' are the charge and flux of the memristor since equation (1) and (2)

coincide with the formula relating charge to current, and flux to voltage, respectively. Hence, Memristor is either charge controlled or flux controlled. Its constitutive relation can be expressed as :

$$\varphi = \hat{\varphi}(q) \quad (3)$$

$$q = \hat{q}(\varphi) \quad (4)$$

Here $\hat{\varphi}(q)$ and $\hat{q}(\varphi)$ are continuous and piecewise differentiable functions charge and field with bounded slopes.

Taking the derivative of eq. (3), we obtain :

$$\frac{d\varphi}{dt} = \frac{d\hat{\varphi}(q)}{dq} \frac{dq}{dt} \quad (5)$$

It leads to

$$v(t) = \frac{d\hat{\varphi}(q)}{dq} i(t) \equiv M(q)i(t) \quad (6)$$

Where, $M(q)$ is a charge controlled memristance defined as :

$$M(q) = \frac{d\phi(q)}{dq} \text{ at } q=q_0 \quad (7)$$

From above equation (7), $M(q)$ can be interpreted as the slope at an operating point $q = q_0$ at time t on the memristor ϕ - q curve. Since the memristance depends on the operating point $q = q_0$ and $q = q_0$ remains fixed when $v(t) = 0$ and $i(t) = 0$, the device can be used as nonvolatile memory. Thus, the resistance $M(q)$ is called the memristance.

2. MEMRISTOR MODELS

All of the memristor models are described in (Iwan Zilinka, 2016) [2]. In this paper a brief description of the models are discussed as follows:

2.1 Linear Ion Drift Model

In the linear ion drift model [3], the actual memristance depends upon the ratio between the value of the dynamic state variable $w(t)$, representing the thickness of the oxygen deficient titanium dioxide layer (TiO_{2x}) and the device thickness D . This model assumes that the vacancies are free to move around the entire length of the device. But it is not true, since the vacancies slow down at the boundary because if they move through the entire device, it means that there will be no physical oxygen vacancies in the device and the length of the doped region is zero. Hence to overcome the boundary problem some window function is adopted.

2.2 Nonlinear Ion Drift Model

In the non linear ion drift model [4], a voltage controlled memristor exhibiting a nonlinear dependence between the voltage and the internal state derivative is assumed. In this model, the state variable w is a normalized parameter within the interval $[0,1]$. This model also assumes a asymmetric switching behavior.

2.3 Simmons Tunnel Barrier Model

The Simmons tunnel Barrier model [5] assumes nonlinear and asymmetric switching behavior due to an exponential dependence of the movement of the ionized dopant, namely, changes in the internal state variable. In this model rather than two resistors in series as in the linear ion drift model, there is a resistor in series with an electron tunnel barrier. The state variable x is the Simmons tunnel barrier width.

2.4 TEAM Model

The TEAM model is a general memristor model [6]. In this model, a current threshold and a tunable nonlinear (polynomial) dependence between the current and derivative of the internal state variable is assumed. The current voltage relationship can be in a linear or exponential manner. It is possible to fit the TEAM model in Simmons tunnel barrier model or to any different memristor model and gain a more efficient computational time with sufficient accuracy.

3. SPICE MODELING OF MEMRISTOR

In a current controlled memristor, the memristor R depends only on charge,

$$V_M = R(q(t))I \quad (8)$$

With the charge related to the current via time derivative $I = dq/dt$. Various models of memristor, a popular model is based on the assumption that the memristive device consists of two regions (of a low and high resistance) with a moving boundary. The total memristance can be written as a sum of resistances of two regions

$$R(x) = R_{on}x + R_{off}(1-x) \quad (9)$$

Here, x parameterizes the position of boundary, and R_{on} and R_{off} are limiting values of memristance. The equation of motion for x with a window function $W(x)$ is as follows

$$\frac{dx}{dt} = kW(x)I, \tag{10}$$

Where k is a constant and W (x) is

$$W(x) = 1 - (2x - 1)^{2p} \tag{11}$$

where, p is a positive integer number.

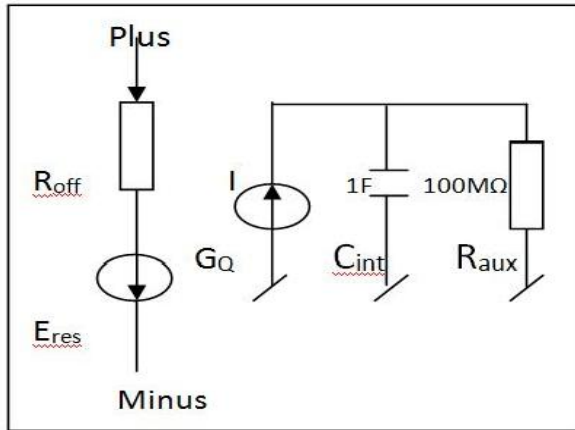


Fig.1: Spice Model of Memristor

Results of fig 2 and fig 3.2 shows the simulation result for the HSPICE model of memristor as shown in fig 1.

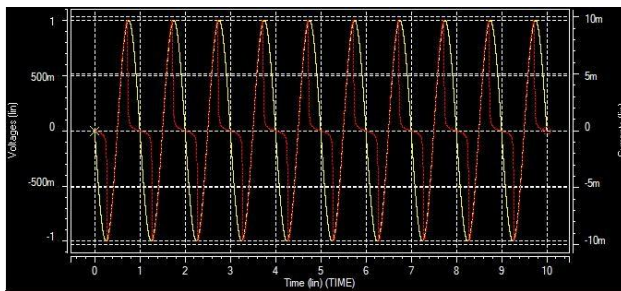


Fig.2: Voltage and Current Waveforms

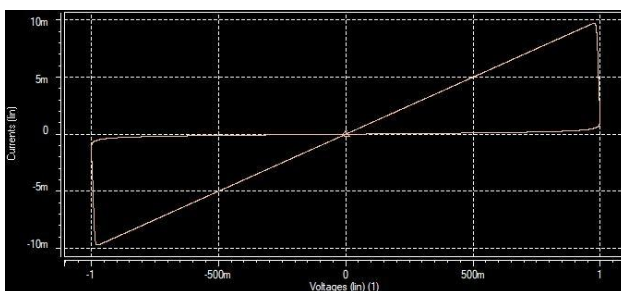


Fig.3: $v - i$ Characteristic of the Memristor. Plot shows pinched hysteresis.

4. MEMRISTOR CIRCUIT

Memristor is a bipolar device hence it can be connected according to its terminal polarities. Serial Memristor Circuit with same polarities - when an input voltage is applied to two serially connected memristors with the polarity as shown in fig 4 & 5.



Fig.4: Series connection with same polarity

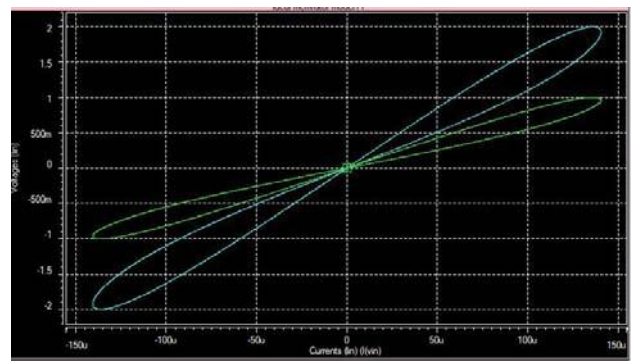


Fig.5: Simulation of Memristor connected in series with same polarity

Serial Memristor circuit with opposite polarity – when an input voltage is applied to two serially connected memristors with the polarity as shown in fig 6 & 7.



Fig.6: Series connection with opposite polarity

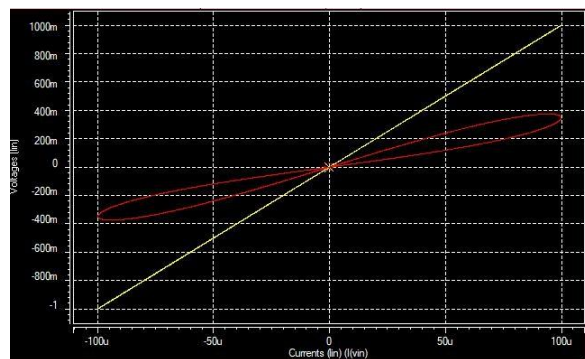


Fig.7: Simulation of Memristor connected in series with opposite polarity

Parallel Memristor Circuit with same polarities - when an input voltage is applied to two parallel connected memristors with the polarity as shown in fig. 8 & 9.

Parallel Memristor circuit with opposite polarity – when an input voltage is applied to two parallel connected memristors with the polarity as shown in fig. 10 & 11.

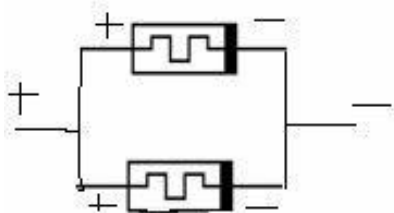


Fig.8: Parallel connection with same polarity

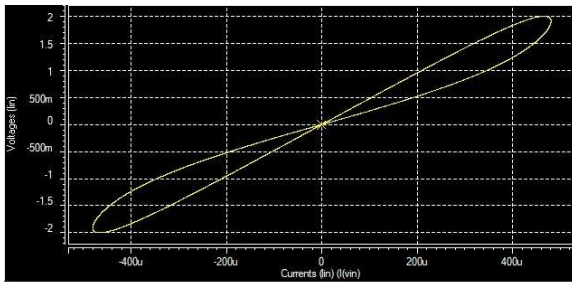


Fig.9: Simulation of memristor connected in series with same polarity

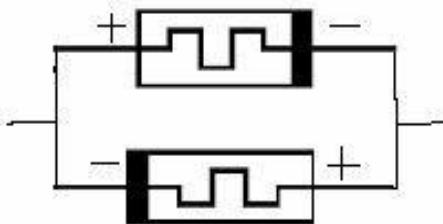


Fig.10: Parallel connection with opposite polarity

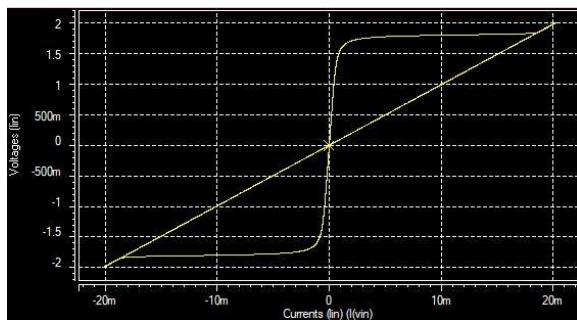


Fig.11: Simulation of memristor connected in parallel with opposite polarity

5. CONCLUSION

The different models of Memristors and a SPICE model specifying its fundamental property of pinched loop hysteresis is introduced.

Then, the different series and parallel combination of memristors are simulated. The series and parallel connected behaves as a composite memristor, provided they have same device parameters.

ACKNOWLEDGEMENT

All authors would like to thank Integral University, Lucknow for providing the manuscript number IU/R&D/2017-MCN000227 for the present research work

REFERENCES

- [1] L. O. Chua, "Memristor: the missing circuit element," *IEEE Trans. on Circuit Theory*, vol. 18, no. 5, pp. 507-519, 1971.
- [2] S. Kvatinsky, "Models of Memristor for SPICE simulation" *IEEE 27th Convention of Electrical and Electronics Engineers in Israel*, vol. 27, pp 213-218, 2012.
- [3] Nalluri, S. K., & Parasaram, V. K. B. (2015). Automating Software Builds with Jenkins: Design Patterns and Failure Handling. *International Journal of Technology, Management and Humanities*, 1(01), 16-33.
- [4] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: ThrEshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2012
- [5] E. Lehtonen and M. Laiho, "CNN Using Memristors for Neighborhood Connections," *Proceedings of the International Workshop on Cellular Nanoscale Networks and their Applications*, pp. 14, February 2010.
- [6] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. S. Williams, "Switching Dynamics in Titanium Dioxide Memristive Devices," *Journal of Applied Physics*, Vol. 106, No. 7, pp. 16, October 2009.
- [7] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: ThrEshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2012
- [8] Z. Bielek, D. Bielek, and V. Biolkov'a. SPICE model of memristor with nonlinear dopant drift. *Radioengineering J.* , 18(2):211, 2009b.